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Evaluation of an un-regulated input isolated DC–DC converter using WBG devices

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Abstract: The paper presents the design and analysis of an un-regulated isolated DC–DC converter using wide band gap (WBG) devices for low-voltage, high current applications. Un-regulated isolated DC–DC converter uses a passive rectifier stage at the front end to connect to the utility grid. This will have a voltage stress of 480–780 V DC at the input of the isolated DC–DC converter. For the evaluation, SiC devices are used at the primary side and GaN devices at the secondary side of the converter. Later on the conclusion, a regulated isolated DC–DC converter, which uses an active PFC at the front-end, will be recommended for having less chip area utilisation, less components and efficient magnetics as far as DC–DC converter is concerned.

1 Introduction

Power supply systems for low-voltage, high current applications such as battery chargers for electric vehicle, magnet power supply etc usually have a front-end AC–DC converter followed by an isolated DC–DC converter. Galvanic isolation is often required between the utility grid and the load for safety and electromagnetic compatibility [1]. So an isolated DC–DC converter is used due to high power density and high efficiency [2–4].

The isolated DC–DC converter can be also with regulated input when they are connected to an active PFC rectifier stage, they can have a regulated input voltage of 900 V DC:

The converter topology, design of magnetics, and selection of various commercially available WBG devices and presented here.

The block diagram of a power supply system with a passive rectifier stage and an un-regulated input isolated DC–DC converter is shown in Fig. 1.

![Block diagram of a power supply system with an unregulated input isolated dc-dc converter](image)

**Fig. 1** Block diagram of a power supply system with an unregulated input isolated dc-dc converter

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>output power, $P_o$</td>
<td>5 kW</td>
</tr>
<tr>
<td>input voltage, $V_{in}$</td>
<td>480–780 V (nominal 560 V)</td>
</tr>
<tr>
<td>output voltage, $V_{out}$</td>
<td>0–100 V</td>
</tr>
<tr>
<td>output current, $I_{out}$</td>
<td>0–50 A</td>
</tr>
</tbody>
</table>

Table 1 Converter specification for un-regulated input

The converter has an output voltage of 0–100 V and current of 0–50 A.

The specification of the un-regulated input isolated DC–DC converter is shown in Table 1.

WBG devices such as SiC and GaN are gaining more and more popular in power converters due to their better performance [5, 6]. The proposed converter utilises WBG devices at both primary and secondary side of the converter. At the input side, the maximum voltage stress on the devices is 780 V. Since high-voltage GaN devices are not available, 1200 V SiC MOSFETs are used at the primary side of the converter. At the secondary side, a 650 V GaN FETS are used. The details will be explained in the further sections.

This paper is intended to have an evaluation of an un-regulated DC–DC converter with respect to the high efficiency magnetic selection and device choice. The paper is organised as, initially, the topology selection of the converter is explained, followed by the selection of various WBG devices and the transformer selection. Later, the switch efficiency curve of the converter is analysed with various commercially available WBG devices and presented here.

2 Un-regulated isolated DC–DC converter

For the converter design with 480–780 V input and 100 V output, full-bridge topology is the best choice for the primary side. At the secondary side, various topologies such as full-bridge [6–8], split-secondary [9, 10], current doubler [11–13], two parallel secondary full bridge are considered. Most of the above-mentioned topologies will use excessive devices in parallel, due to the current requirement at the secondary side, which will have more losses and the sharing of the current between the parallel devices will be a big challenge. Fig. 2 shows the proposed converter topology with dual current doubler circuit and using two current sharing transformer [13]. Even though, the proposed converter topology uses two current sharing transformer, it reduces the excessive paralleling of 650 V GaN devices. For the proposed converter design, two 650 V GaN devices will be used in parallel at each switch on the secondary side of the converter.

The switching waveforms of the converter along with the PWM signal for each switches are shown in Fig. 3. At the primary side of the converter, diagonal switches (S1.1 & S1.2 or S1.3 & S1.4) are controlled by the same PWM signal and are 180° phase shifted to the other diagonal PWM signal (S1.3 & S1.4 or S1.1 & S1.2). At the secondary side, the switches S2.1 and S3.1 are controlled from the same PWM signal. Similarly, the switches S2.2 and S3.2 are also controlled by the same PWM signal. Two current sharing
the transformer core has to be increased. So, for the evaluation of the proposed converter, the switching frequency of the converter is selected as 200 kHz. Compared to Si devices, SiC and GaN devices will also have lower capacitive switching losses even at 200 kHz [15].

The maximum voltage on the secondary side switches will be 340 V, and the only commercial available high-voltage GaN FETS are 650 V, they are been selected for the secondary-side switches.

The current transformer mentioned in the circuit can be extremely small; it is only supposed to take the small imbalances in the paralleled circuit. The losses from the two current transformer is not accounted for the evaluation of the proposed converter.

3.1 Transformer

In order to design a high efficiency compact transformer, selection of proper core material and windings are crucial. Ferrite materials have been a proper choice for high-frequency transformer for many decades due to their high electrical resistivity and low eddy current losses [15]. Since, Ferroxcube 3C95 shows a flat power loss density variation with temperature, they are selected as the core material [16].

Two planar transformers are used to realise the converter. Primary side of the transformer is connected in series and the secondary side is connected in parallel.

The core loss is calculated using the Steinmetz formula [17],

\[
P_v = k f^\alpha B^\beta
\]

where \( P_v \) is the power loss per unit volume, \( B \) is the flux density and \( f \) is the frequency. \( k, \alpha, \beta \) are the Steinmetz parameters of the magnetic material.

The copper loss can be approximately calculated from the winding resistance of the transformer and the RMS current through them. The primary current in the transformer will be \( \frac{1}{4} \) of the output current due to two parallel current doubler circuit at the secondary side. Transformer primary RMS current can be given by the equation, assuming constant inductor current,

\[
I_{RMS,hi} = \frac{I_f}{4} \sqrt{2} D
\]

The specification of the two transformers with the loss values at full load is tabulated in Table 2.

The AC-resistance of the transformer windings is also important for the calculations of copper losses, due to the high switching frequency as well. For the ease of calculations, it is difficult to estimate the resistance factor for planar transformer and it is not included in the evaluation. So, the copper losses can be much higher than the expected value.

3.2 Switching devices

As mentioned, WBG devices will be utilised both at the primary side and secondary side of the converter. 1200 V SiC MOSFETs are used at the primary side and 650 V GaN FETS (two in parallel) are used at the secondary side.

Conduction loss at both the primary-side switches and secondary-side switches can be calculated from the respective switch on-resistance and the RMS current through them.

\[
P_{ON,ps} = I_{RMS,SS} R_{DS,ON,ps}
\]

\[
P_{ON,ss} = I_{RMS,PS} R_{DS,ON,SS}
\]

Due to two parallel current doubler circuit, the current seen by individual device is \( \frac{1}{4} \) of the output current. The RMS current in the primary-side and secondary-side switches can be given by the expression, assuming a constant inductor current.

\[
I_{RMS,ps} = \frac{I_f}{4} \sqrt{2} D
\]
on-resistance device will have lower output capacitive charge and converter on-resistance are used in parallel at each switch configuration in MOSFETs are compared, which have almost the same total loss at combination of 1200 V SiC MOSFET #1 at the primary switch and two parallel 650 V GaN FETs are dependent on the output capacitive charge of the devices. High on-resistance is from the output capacitive charge of the device. The capacitive switching loss of the primary-side and secondary-side switches can be calculated as \[ P_{\text{loss,PS}} = \frac{2Q_{\text{V}_{\text{in}}}}{V_{\text{in}}/2} f_{\text{sw}} \] (7) \[ P_{\text{caploss,SS}} = 2Q_{\text{V}_{\text{in}}}/3V_{\text{in}} f_{\text{sw}} \] (8) \[ Q_{\text{loss}(V)} = \int_0^V \frac{C_{\text{cap}}(v)}{V_{\text{in}}/8} dv \] (9) where \( Q_{\text{V}_{\text{in}}} \) is the output charge of four parallel primary switches at \( V_{\text{in}} \). \( Q_{\text{V}_{\text{in}}} \) is the output charge of primary switches at \( 5V_{\text{in}}/8 \). \( Q_{\text{V}_{\text{in}}} \) is the output charge of two parallel secondary switches, \( V_{\text{in}} \) is the input voltage of the converter, \( f_{\text{sw}} \) is switching frequency, and \( n \) is the turns ratio of the transformer. 

At the primary side of the converter, three potential 1200 V SiC MOSFETs are compared, which have almost the same total loss at full load. At the secondary side, two 650 V GaN FETs with 27 mΩ on-resistance are used in parallel at each switch configuration in the topology. 

Table 3 shows the conduction loss and switching loss, at full load condition, for the primary-side switches and secondary-side switches, which are calculated from (3), (4) and (7), respectively. 

For a MOSFET, the on-resistance corresponds to the conduction loss in the switches. The losses from switching at certain frequency are dependent on the output capacitive charge of the devices. High on-resistance device will have lower output capacitive charge and thereby lower switching loss and vice versa. This can be clearly seen in Table 3. 

Fig. 4 shows that the switch efficiency curve for the converter with various primary SiC MOSFETs. From the figure, the combination of 1200 V SiC MOSFET #1 at the primary switch with two parallel 650 V GaN FET at the secondary side is a best combination. At full-load condition, they still have almost same losses as the other two combination, but this combination will have lower switching loss, which means higher efficiency at light load condition. 

The 1200 V SiC MOSFET with still higher on-resistance (above 75 mΩ) is not been chosen for the comparison because after this on-resistance, the conduction loss will be much higher and the switching loss will be almost negligible. Higher conduction loss will have low efficiency at higher load conditions and after a certain power level, the thermal dissipation will be much higher and discrete devices may not able to handle the heat.

From a DC–DC converter point of view, a regulated DC–DC converter can be advantageous compared to an un-regulated DC–DC converter, this topic has to be further investigated and will be available in future publications. 

Regulated converter is connected with an active PFC circuit at the front end, which can boost the voltage to 900 V before feeding to the DC–DC converter. Such converter can work with a single transformer with a high turns ratio (1:8). For a 100 V output, a 200 V GaN FETs can be used at the secondary side. 

A full-bridge forward converter can be used as the topology for such regulated DC–DC converter. From the calculations for the regulated DC–DCc converter (not explained here due to space constrains), the efficiency can be higher for magnetic components. 

This also reduces the usage of two current sharing transformer. A double switching frequency inductor can be used at the output of the converter.

The chip area of the 200 V GaN FET is much smaller than 650 V GaN FETs, so by using low-voltage devices for the design, the chip area can be reduced for a regulated input DC–DC converter. Chip area implies cost of the devices, i.e. a regulated input DC–DC converter can be cost-efficient compared to an un-regulated input DC–DC converter. Future publications can be expected in this topics for comparison of an un-regulated and regulated input isolated DC–DC converter.

4 Conclusion

This paper is presented to have an evaluation of un-regulated input isolated DC–DC converter for a power supply system. The converter utilises a passive rectifier circuit at the input of the un-regulated input isolated DC–DC converter. The voltage stress on the input primary devices can vary from 480—780 V DC. For the evaluation of the converter, 1200 V SiC MOSFETs are used. For the primary side and at the secondary side 650 V GaN FETs are used. Such a converter uses two planar transformer with input side in series for high input voltage and uses parallel windings to have high current capability at the secondary side of the converter. The switch efficiency curve of the converter with various 1200 V SiC MOSFETs are compared and presented in the paper.

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6 References


