High Efficiency Three-phase Power Factor Correction Rectifier using Wide Band-Gap Devices

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High Efficiency Three-phase Power Factor Correction Rectifier using Wide Band-Gap Devices

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Dedicated to my wife Farideh for her endless love and support & to my priceless parents.
Preface

This thesis presents the work that author has carried out at faculty of Engineering, University of Southern Denmark. This PhD project has started since December 2013 and finished in November 2016. The thesis is submitted in partial fulfilment of the requirements for obtaining the PhD degree. The general structure of this thesis is based on the published papers that author has done during the PhD program.

This project is part of the Intelligent Efficient Power Electronics (IEPE) research center. IEPE is a strategic research center between three universities- University of Southern Denmark, Aalborg University, and Technical University of Denmark- and four Danish leading high technology companies- Danfoss Drives, Grundfos A/S, KK Electronics, and Vestas. The main objectives of IEPE are new hardware design methods, new device technologies, increasing the conversion efficiency of the power electronics converters. Being part of the big and sophisticated project such as IEPE gave the author this opportunity to start a constructive collaboration with companies in line with the objectives of the project in Denmark, especially Danfoss Drives A/S. The collaboration which has been conducted during the PhD work under IEPE agreement has led to valuable technical achievements and personal experiences.

This specific PhD project was part of the platform demonstrator known as a three-phase adjustable speed drives for motor and pumps which was led by Danfoss Drives A/S. As a result, the project was productively connected to the activities at Danfoss Drives to reach to the main goal of the work package. The main goal is connecting the power factor correction rectifier to the variable speed drive in kW range using wide-band gap devices. Therefore, part of the project as a plan was conducted in Danfoss Drives laboratory. In this regard, Danfoss Drives A/S cooperation was outstanding throughout the last 9 months of the project. Author would like to thank Danfoss Drives for their support, especially from Niels Gade, Andreas Aupke, Radu Lazar, Marian Lungeanu, Marco Zucherato, and many others from Danfoss that gave the author lots of thoughts and technical tips.
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I owe a great debt of gratitude to Radu Lazar from Danfoss Drives A/S. His support, his knowledge, and his impressive delicacy and skill were definitely a key for finishing this project. Working with Radu not only improved my technical understanding but also taught me to be always hopeful and trying to do the best.

I would also like to present my gratitude to Prof. Stephen Dodds for his precious time and his valuable comments on my thesis.

I am very thankful to have a good working environment and would like to thank all my colleagues and friends at SDU. I would also like to give my special appreciation to all the former and present colleagues at the Maersk Mc-Kinney Moller Institute especially to Rakesh Ramachandran, Fazel Taeed, Ishtiyaq Ahmed Makda, and Karsten H. Andersen.

My special thanks to Jesper Nielsen for helping me with PCB and his great effort to realize the hardware prototypes of the converter.

My colleague and my wife, Farideh Javidi! Without your support, your understanding, your sacrifices and your love I would never be able to finish this work. Thank you for being with me and giving me the energy to be the best.

And finally, I would like to thank all my family members and friends, too numerous to name, for their encouragement and great support, without whom the successful completion of this thesis would not have been possible.

I would like to thank my incredible parents for giving me their endless love, by my mother language, Persian:

پدرم، مادرم از آنجام پاسخ‌هایی که بی‌رحمانه به خاطر بی‌رحمانی‌های خود بانی‌البنا، دانشگاه‌هایی را که می‌شناسند، و دانشگاه‌هایی که به تدریس کاربردی کارکردی، نمی‌پردازند. با آن‌ها تا زمینه‌ای شامل کار کاربردی گردیده‌ام.

مبارک
Abstract

Improving the conversion efficiency of power factor correction (PFC) rectifiers has become compelling due to their wide applications such as adjustable speed drives, uninterruptible power supplies (UPS), and battery chargers for electric vehicles (EVs). The attention to PFCs has increased even more since grid regulations have become stricter in terms of injected harmonic and power quality. Therefore, improving the efficiency and the power quality of PFCs are the main objectives of this PhD work.

New wide band gap (WBG) power switches have better switching characteristics in comparison with silicon power devices. Therefore, the PFC switching frequency using WBG devices can potentially be increased. This advantage helps the reactive components to be reduced in size. However, it also brings challenges such as identifying a proper material for inductive components that has lower loss and layout design that has lower parasitic elements. To fulfill the grid regulations (e.g. IEEE-519) high order filters are normally used. Achieving an optimum filter design is vital for having an efficient converter. Reducing low frequency harmonics can improve both the efficiency and also the power quality. Therefore, current controllers are also important to be investigated in this project.

In this PhD research work, a comprehensive design of a two-level three-phase PFC rectifier using silicon-carbide (SiC) switches to achieve high efficiency is presented. The work is divided into two main parts: 1) Optimum hardware design using WBG devices to improve the conversion efficiency and 2) Identifying the impact on the efficiency by current controller.

Part 1 is presented in Chapter 3. The converter topology is a two-level bidirectional boost voltage source converter (VSC). SiC devices (i.e. MOSFET and diode) are used for designing the converter. An analytical method for choosing the filter parameters to achieve an optimum design is presented. The method is based on the working principle of the converter. It focuses on analyzing the converter current and voltage for generalizing the filter design. The switching frequency which leads to the maximum converter efficiency is analyzed and selected. According to the selected switching frequency, an optimum LCL filter is designed and the layout is optimized for a 5 kW three-phase PFC using SiC MOSFETs.

The second part is presented in Chapter 4. It is focused on current controller and its impact on the efficiency. Two types of current controllers are studied: PI current controller in the rotational reference frame and proportional-resonant (PR) current controller in the stationary reference frame. For the PR controller, harmonic compensation is employed to improve the power quality. To have similar harmonic performance the PI controller needs larger filter in comparison with the PR controller. This eventually ends up with lower efficiency of the converter with the PI current controller.

In this thesis, two sets of experiments are carried out:

- Verification of the designed filter and the controllers performance in Chapter 3 and Chapter 4, respectively;
• Measurement and comparison of the converter efficiency for two types of controllers.
The highest efficiency is achieved at 50% of nominal load for the PR current controller. The measured efficiency is 99.1% at 50% of nominal load and 98.95% at full load. The converter with the PR controller is more efficient than the converter with the PI controller at low load.
Resumé

Det er blevet interessant at optimere konverterings effektiviteten af Power factor Controllere (PFC) pga. deres store udbredelse inden for motordrives, nødstrømsanlæg (UPS) og batteriladere til el biler (EVs). Der er øget fokus på PFCere på grund af strengere regler for ledningsbåret harmonisk støj og strømkvalitet på lysnettet (Grid). Derfor er det primære mål med denne PhD at øge effektiviteten og strømkvalitet.

Pga. switching karakteristikken på de ny wide band gap (WBG) halvleder komponenter, kan switching frekvensen øges i forhold til de traditionelle silicium (Si) baserede PFCere. Den øgede switch frekvens muliggør design af mindre reaktive komponenter. Dette medfører også nye udfordringer såsom at finde egne materialer til de induktive komponenter som har lavere tab og lave et print layout med minimal parasitiske elementer. For at opfylde regulativerne for lysnettet (f.eks. IEEE-519) benyttes traditionelt højere ordens filtre. At opnå et optimalt filter design er vitalt for at have en effektiv konverter. Reduktion af lavfrekvent harmonisk støj kan både forbedre effektiviteten og strøm kvaliteten. Derfor er strøm kontrollerer også vigtige og vil blive undersøgt i dette projekt.

I denne PhD afhandling bliver et omfattende design af en højeffektiv two-level 3 faset PCF som benytter siliciumkarbid (SiC) switching komponenter præsenteret. Den er opdelt i to hoveddele. 1: Optimal hardware design ved brug af WBG, for at forbedre konverteringseffektiviteten. Og 2: Identificere strømkontrollerens indflydelse på konverteringseffektiviteten.


Anden del bliver præsenteret i kapitel 4. Her bliver der fokuseret på strømkontrollens indflydelse på effektiviteten. Der bliver undersøgt to forskellige typer kontrollerer: Proportional-Integral (PI) strømkontrollerer i det roterende reference system og proportional-resonans (PR) strømkontrollerer i det faste reference system. For PR kontrolleren implementeres harmonisk kompensering for at forbedre strømkvaliteten. Når PI kontrolleren benyttes skal konverteren have et større filter end når PR kontrolleren benyttes for at opnå samme harmoniske egenskaber. Dette medfører at koncerten har en lavere effektivitet end med PI kontrolleren.

I denne afhandling er der blevet udført to eksperimenter:

- Verifikation af det designede filter (kapitel 3) og kontrollerens ydeevne (kapitel 4).
Måling og sammenligning af konverterens effektivitet med de to typer kontrollere. Den højeste effektivitet er målt ved 50% af den nominelle belastning med PR kontrolleren.

Den målte effektivitet er 99,1% ved 50% belastning og 98,95% ved fuld belastning. Konverteren med PR kontroller er mere effektiv ved lav belastning end konverteren med PI kontroller.
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Abbreviations

ADS       Adjustable speed drives
ANPC      Active Neutral Point Clamped
CHB       Cascaded H-Bridge
CCM       Continuous conduction mode
DSOGI     Dual second order generalized integrator
EV        Electric vehicle
FC        Flying capacitor
FFT       Fast Fourier transform
GaN       Gallium-Nitride
HC        Harmonic compensation
HGNPC     Hybrid Generalized Neutral Point Clamped
mmf       Magneto motive force
MOSFET    Metal Oxide Semiconductor Field Effect Transistor
MPP       MolyPermalloy powder cores
NPC       Neutral point clamped
PCB       Printed circuit board
PFC       Power factor correction
PWM       Pulse width modulation
Si        Silicon
SiC       Silicon-Carbide
SJ        Super junction
SOGI      Second order generalized integrator
SPWM      Sinusoidal Pulse width modulation
SVM       Space vector modulation
THPWM     Third-Harmonic PWM
UPS       Uninterruptible power supply
VSC       Voltage source converter
WBG       Wide-band gap
Nomenclature

\( \Delta i \)  
Converter current ripple

\( \Delta V_{\text{ripple}} \)  
AC voltage ripple of filter capacitor

\( \theta_{\text{comp.}} \)  
Compensated phase delay

\( \theta_i \)  
The angle of the converter current

\( \theta_{i,delay} \)  
The delay introduced to the measured converter current

\( \theta_V \)  
The angle of the PCC voltage

\( \theta_{V,delay} \)  
The delay introduced to the measured PCC voltage

\( \lambda \)  
Delay

\( \omega_g \)  
Fundamental angular frequency of grid

\( \omega_{\text{sw}} \)  
Angular frequency of switching

\( C_d \)  
Damping filter capacitance

\( C_{d,max} \)  
Maximum damping filter capacitance

\( C_{d,min} \)  
Minimum damping filter capacitance

\( C_{\text{dc}} \)  
DC link capacitance

\( C_f \)  
Filter capacitance

\( C_{\text{oss}} \)  
Output switch capacitance

\( f_g \)  
Grid frequency

\( f_{\text{res}} \)  
Resonant frequency of the filter

\( f_{\text{sw}} \)  
Switching frequency

\( g_{cc} \)  
Gain of the feedforward voltage

\( h \)  
The harmonic number

\( I \)  
Converter current

\( I_c \)  
Filter shunt current

\( I_D \)  
MOSFET Drain current

\( I_g \)  
Grid current

\( I_{\text{load}} \)  
Load current (DC)

\( K_{\text{cos},h} \)  
The compensation gain for \( h^{th} \) harmonic on the path of \( \alpha \)-axis

\( K_i \)  
Integral gain of the current controller

\( K_{i,h} \)  
Integral gain of the \( h^{th} \) harmonic compensator

\( K_P \)  
Proportional gain of the current controller

\( K_{P,dc} \)  
Proportional gain of the dc link controller

\( K_{\text{sin},h} \)  
The compensation gain for \( h^{th} \) harmonic on the path of \( \beta \)-axis

\( L_c \)  
Converter-side inductance

\( L_f \)  
Grid-side filter inductance

\( L_{\text{grid}} \)  
Grid inductance
$L_T$ Total series inductances of the filter
$m_3$ Modulation index of the injected third harmonic
$m_a$ Modulation index
$P_{cap}$ MOSFET capacitor loss
$P_{Cond.}$ Switch conduction loss
$P_{copper}$ Total copper loss
$P_{core}$ Inductor core loss
$P_{drive}$ MOSFET drive power
$Q_{oss}$ Output switch charge
$Q_G$ MOSFET gate charge
$R_d$ Damping resistor
$R_{dc}$ DC copper resistance
$R_{DS}$ MOSFET drain source resistance
$R_{LISN}$ LISN resistance
$R_{load}$ Load resistance
$R_T$ Total series resistances of the filter inductances
$S$ Apparent power
$I_{i,dc}$ Integral gain of the dc link controller
$T_{in}$ Inner time of dc voltage control loop
$T_s$ Sampling time
$T_{sw}$ Switching period
$V_{an}$ Converter voltage
$V_b$ Base voltage
$V_{dc}$ DC link voltage
$V_{drive}$ MOSFET drive voltage
$V_{DS}$ MOSFET drain source voltage
$V_{ff}$ Feedforward voltage
$V_m$ Peak of voltage at point of common coupling (PCC)
$V_{PCC}$ Voltage at PCC
$V_{aN}$ AC link voltage of phase $x$
$Y_{eq}$ Equivalent admittance
$Z_b$ Base impedance
$Z_{grid}$ Grid impedance
1. Introduction

This thesis is to present the results obtained in the PhD project entitled as “high efficiency three-phase power factor correction using wide band-gap devices” performed by the author from December 2013 to November 2016. Many scientific results obtained in this project have been published in peer reviewed journal and conference papers. The published papers are included in Appendix B1-Appendix B8.

The main target of this report is to place the published papers in the context of the project objectives and present a more coherent and complete overview of the work carried out over three years.

It is intended that this thesis can serve as a design aid for three-phase power factor correction rectifiers: Hardware and Control for achieving relatively high conversion efficiency compared with the current state-of-the-art.

1.1. Background and Motivation

Three-phase ac-dc converters are widely used in adjustable speed drives (ADS), uninterruptable power supplies (UPS), high voltage dc systems (HVDC), battery energy storage systems, battery charger for electric vehicles (EVs), and power supplies used in telecommunications. Conventional ac-dc converters, line-commutated rectifiers, are highly non-linear and introduce high level of grid current harmonics and low power factor. Traditionally, passive filters are used to reduce the current harmonics and improve the power quality of the ac side. However, this solution requires a bulky passive filter which reduces the conversion efficiency [1]-[4].

The international regulations, in term of power quality, have forced power electronics and power systems engineers to develop active solutions. A new breed of rectifiers using new solid-state force-commutating devices such as MOSFETs and IGBTs bring the following advantages: (a) the current or voltage can be modulated, generating a smaller harmonic contribution; (b) the power factor can be controlled; and (c) they can be built as voltage source or current source rectifiers [1]-[4]. Such converters are generally identified using different terms such as switched-mode rectifiers, power factor correction rectifiers (PFC), and pulse width modulation (PWM) rectifiers. In this thesis, the term PFC is used as a general name for such converters.

Recently, many promising PFC topologies using force-commutated devices have been proposed and this topic has become an active research topic in power electronics due to the PFCs unique characteristics. Three-phase two-level boost PFC is able to achieve the best performance in terms of shaping the input current and allowing bidirectional power flow with a minimum number of active switches [1]-[2].

To improve the conversion efficiency, each component needs to be optimized by both selecting the material and the design. To minimize the loss in the switches, it is reasonable to
use power devices which 1) introduce low on-resistance and 2) have a good transient performance (i.e. low input and output capacitance charge). The first one contributes to reduction of conduction loss and second one in reduction of switching loss.

Currently, the power semiconductor devices are based on the mature and well-established silicon technology. However, silicon exhibits some limitations in terms of blocking capability, thermal conductivity, capacitive charge, and saturated drift velocity [5]. Instead, wide band-gap (WBG) technology becomes highly attractive compared to Si technology because of their low switching losses, low conduction loss, high temperature capability. Among the possible candidate silicon-carbide (SiC) and gallium-nitride (GaN) present better tradeoff between the theoretical characteristics and the real commercial availability [5]-[7]. The improved switching characteristic of WBG devices compared to their Si counterparts means that they may allow shorter switching times. Decreasing the transition time and increasing the switching frequency allows smaller reactive components i.e. capacitors and inductors. Design for higher frequency, however, will introduce new challenges regarding layout design ensuring lower stray inductance for semiconductors and designing better inductor regarding magnetic material and type of winding.

Therefore, passive components, especially inductors are among the most important in PFC converters as they have a high impact on the efficiency and the performance of PFCs. High switching frequency introduces corresponding high frequency current ripple in the PFC inductors. Then analysis of the high frequency minor \( B-H \) loops caused by high frequency current ripple makes core loss calculation even more complicated. The ac copper loss by the skin and the proximity effects can also be a critical issue in designing the inductors to avoid having large copper loss.

It can be concluded that in designing of PFCs either two-level or multilevel configurations, there is a strong non-linear correlation between various parameters and components. For instance, increasing the switching frequency decreases the size of the reactive components. But it increases the switching loss. It may increase the core loss in the magnetic materials, and it increases the ac copper loss. So, there should be a trade-off between these parameters. There is an optimum point that the maximum efficiency is achieved. This PhD project provides an answer to this question: through emerging high frequency WBG devices, thereby revealing possible ways to increase the efficiency of three-phase PFCs?

1.2. Project objectives and Contributions

1.2.1. Research objectives and challenges

The primary objectives of the project are as follows:

- Increasing the conversion efficiency of a 5-10 kW three-phase power factor correction rectifier;
- Improving the power quality of the converter;
- Providing bidirectional power flow;
CHAPTER I - INTRODUCTION

The primary topology for PFC is a two-level voltage source converter (VSC) using SiC switches. Accordingly, the challenges towards the main objectives of the project are addressed as follows:

- To present a general and straightforward method for designing the converter-side inductor and calculating its power loss;
- To identify a core material for the inductor that yields a relatively low core loss;
- To derive a general design method to optimize the ac line filter based on the principle of operation of the converter;
- To design a layout for the high frequency SiC switches that minimizes the parasitic elements in the circuit;
- To identify better controller for PFC which has more impacts on the efficiency;
- To identify possible improvements that wide band-gap devices bring for PFC converters.

1.2.2. Contributions

The contribution of this work can be split in two categories:

1) Design methodology

- A general method for choosing and designing the converter-side inductor has been established;
- A general method for calculating core and copper losses for the converter-side inductor (i.e. the boost inductor) is derived;
- A comparison of three wire and four wire PFC has been made regarding the achievable efficiency;
- A general method for calculating the parameters of the ac line filter to minimize its size and/or maximize its efficiency has been derived;

2) Control methodology

- The impact of feedforward compensation in control methods has been studied;
- The impact of two common control methods on the efficiency has been investigated.
1.3. Thesis overview

The thesis includes an extended summary and a collection of the published and submitted scientific papers. Parts of the papers are used directly or indirectly in the extended summary of the thesis. The purpose of this thesis is, therefore, to complement the already published papers by providing a coherent presentation of the overall project and its results. Special focus will be devoted to present a coherent derivation of the key fundamental theoretical aspects of this project.

Since most of the experimental results are presented in the published material reproduced Appendix B, only summaries of the results are given in the main body of the thesis with the main purpose of extending the analysis of the experimental results to verify the validity of the theoretical results. The content and structure of the thesis is depicted in Fig. 1.1.

In Appendix A, the next step of the project is briefly explained. The next step will be on using commercially available GaN switches for PFC rectifier on the basis of multilevel converters. In this appendix, the principle operation of the converter is explained and the design process is optimized by following the same path for two-level PFC as explained in Chapter 3 and 4. The inductor will be designed for the converter using the general approach which is presented in Chapter 3. The layout design in this case will be more complicated in comparison with the two-level PFC. The converter is a 10 kW hybrid three-level three-phase active neutral point clamped (ANPC) which utilizes both GaN and Si switches. In this case, several challenges is addressed and studied as follows:

- To identify a suitable topology which utilizes the best out of GaN switches which are commercially available;
- To design a proper layout, especially for the GaN drivers;
- To extend the proposed methodology of two-level PFC (Chapter 3 and 4) to the new topology;
- To compare the achieved results of two-level and multilevel with two different technologies of WBG devices, SiC and GaN, respectively.

1.4. List of publications

Many of the scientific results obtained in the project have been published in the form of peer reviewed conference and journal papers. The published papers form an integral part of this thesis and are included in the Appendix B. The list of publications is arranged according to the published year. They are listed as follows:


2. State of the art

The purpose of this chapter is to present an overview of the present state of the art of three-phase PWM power factor correction (PFC) rectifiers/three-phase voltage source converters (VSCs). Recent published literature primarily in the form of journal papers, conference papers and tutorial notes, has been searched and analyzed to establish the state of the art. The main focus has been to identify publications presenting technical results, preferably supported by experimental results and useful for or related to the overall specification defined for this project.

For many years, ac-dc converters have vastly been investigated from different aspects such as topology, switching patterns, control, design at the components level, harmonic analysis, and etc. By emerging the new type of power semiconductors as wide band gap devices, the attention on employing these switches for PFC applications or generally PWM VSCs is increased. Consequently, a significant amount of scientific literature has been published on the subject. To best be able to provide a fair comparison for this study, the following categorization is presented for the state of the art:

- The overall optimization and design of ac-dc converters, which can be two-level or multilevel with different topologies, the focus not being on the topology, but on the conversion efficiency [16]-[29];

- Optimization at the component level including the inductor core material, the boost inductor loss and/or size minimization [30]-[33] and [39]-[44];

- Filter design [45]-[65] and stability of grid-connected converters [66]-[76].

Although, this PhD work utilizes wide-band gap devices for implementation, the focus is not on studying the technology behind these devices but on implementing and comparing the attainable performance with the current state of the art in PFC rectifiers.

Papers published as part of this project are not, of course, included in the state-of-the-art analysis but are attached in Appendix B.

2.1. Three-phase voltage source converters

Most research to date has focused on the efficiency of the converter only considering switching and conduction losses. Unfortunately, very few papers have been published on optimization of the whole converter with respect to high efficiency. Here, papers on efficiency and the supporting experimental results will be discussed.

A 10 kW SiC based three-phase boost PFC with 6 discrete SiC switches has been made and addressed in [16]. The optimum switching frequency is suggested to be 40 kHz. The converter is connected via an \textit{LCL} filter to the grid. The maximum efficiency in the rectifier mode reported in this paper is 98.75\% at half load and 98.65\% at full load for 600 V dc link
voltage. The efficiency in the inverter mode is slightly lower than in the rectifier mode. Fig. 2.1 shows the schematic of a two-level three-phase boost PFC rectifier with an $LCL$ filter.

In [17], a 10 kW two-level three-phase SiC based boost grid-connected converter has been investigated. The converter is designed with an $LCL$ filter for fulfilling the grid regulations. In the design, the three-phase SiC MOSFET module has been used at a switching frequency of 16 kHz. A ferrite core is utilized for the high frequency converter-side inductor. The measured efficiency shows a maximum of approximately 99% around 50% of the nominal load. The dc link voltage is 580 V.

Paper [18] reports the design of a 5 kW fully SiC JFET-based three-phase boost converter operating at 48 kHz. The maximum achieved efficiency is lower than 98%. Increasing the load reduces the efficiency and this reaches a minimum of 97.5% at full load. This paper, however, has not also specified the filter specifications and the associated losses.

Three different 10 kW converters have been designed with various criteria including size and efficiency in [19]. The high efficiency converter design has already been explained in [17]. The minimum size is achieved by increasing the frequency to 80 kHz but the efficiency reduces from 99.1% to 98.2% while the power density increases from 0.94 kW/dm$^3$ to 5.23 kW/dm$^3$.

In [20], one diode at the output of the converter is added to improve reliability and provide zero voltage transition. The test condition for a 5 kW converter using IGBT switches are: 180 V rms input, 350 V dc link output and 50 kHz switching. The maximum efficiency is 97% and the minimum is 96.5%. According to the efficiency curve, it can be said that the converter has been oversized because the maximum efficiency occurs at full load.

![Fig. 2.1: The schematic of a two-level three-phase PFC rectifier with $LCL$ filter.](image-url)
TABLE 2-1: Efficiency comparison of the recent state of the art.

<table>
<thead>
<tr>
<th>Paper</th>
<th>Power</th>
<th>Topology</th>
<th>Switch type</th>
<th>DC link voltage (V)</th>
<th>Switching frequency (kHz)</th>
<th>Peak efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[21]</td>
<td>5 kW</td>
<td>Buck</td>
<td>CoolMOS</td>
<td>400</td>
<td>18</td>
<td>98.8</td>
</tr>
<tr>
<td>[22]</td>
<td>7.5 kW</td>
<td>Buck</td>
<td>IGBT</td>
<td>400</td>
<td>28</td>
<td>98.5</td>
</tr>
<tr>
<td>[16]</td>
<td>10 kW</td>
<td>Boost</td>
<td>SiC MOSFET</td>
<td>600</td>
<td>40</td>
<td>98.75</td>
</tr>
<tr>
<td>[17]</td>
<td>10 kW</td>
<td>Boost</td>
<td>SiC MOSFET</td>
<td>580</td>
<td>16</td>
<td>99</td>
</tr>
<tr>
<td>[18]</td>
<td>5 kW</td>
<td>Boost</td>
<td>SiC JFET</td>
<td>600</td>
<td>48</td>
<td>98</td>
</tr>
<tr>
<td>[19]</td>
<td>10 kW</td>
<td>Boost</td>
<td>SiC MOSFET</td>
<td>350</td>
<td>50</td>
<td>97</td>
</tr>
<tr>
<td>[20]</td>
<td>3 kVA</td>
<td>NPC</td>
<td>SJ MOSFET</td>
<td>720</td>
<td>20</td>
<td>99.3</td>
</tr>
<tr>
<td>[24]</td>
<td>5 kW</td>
<td>Six-pack</td>
<td>SiC MOSFET</td>
<td>650</td>
<td>10</td>
<td>98.5</td>
</tr>
</tbody>
</table>

1The liquid cooling has been used in this converter.
2Six-pack SiC MOSFET module has been used in this design.
3A diode has been put in series at the dc output of the converter.
4Super-junction.
5Only switching device losses.

Paper [21] presents a 5 kW three-phase buck converter with a 400 V dc link voltage. The reported conversion efficiency is 98.8% achieved with CoolMOS with a minimum of 97.6% at 10% of full load.

A 7.5 kW three-phase buck converter with the output dc link voltage of a 400 V has been reported in [22]. The efficiency at full load is 98.5% with a liquid cooling system. The switching frequency is set to 28 kHz using SiC switches. This paper also addresses the ac inductor design including finding a suitable material for the inductor. According to the power rating, inductance size, and the wire size different core materials have been compared. Nano-crystalline core has been suggested for the high frequency inductor.

In [23], a 10 kW T-Type converter has been tested at switching frequency swept between 4-48 kHz. The focus of this paper is on the switching and conduction loss and its comparison with conventional three-phase converters.

TABLE 2-1 summarizes the useful information obtained from the literature search, with focus on the converter specifications and the overall efficiency.

2.2. Optimization on component level: inductor and core material

Optimization of the converter efficiency requires optimization with respect to every component. This section is focused on inductor design for grid-connected PWM voltage source converters (VSCs).

The electrical and thermal performance of the hard switched boost PFC is heavily dependent on the characteristics of the switching devices and boost inductor [30]. Magnetic and inductor design entail trade-offs: a saving in one area can make things worse elsewhere with an overall change in harmonics or efficiency. Thus choosing the optimum is critical for minimizing the
overall loss. Improving the efficiency of the inductor highly depends on core material and inductor winding method.

There are various core materials that are commercially available such as ferrite, powder, powder core, amorphous, Nano-crystalline, and etc. Any of these core materials has different specifications and can be suitable for the PFC inductor according to the power level, current ripple frequency, magnitude of current ripple.

In [31], three different core materials have been compared for the main inductor ($L_c$ in Fig. 2.1) used in two-level three-phase PFCs: i) Ferrite (EPCOS), ii) Amorphous, and iii) Powder core-Kool-M$\mu$. The power rating of the converter is 20 kW and the switching frequency is swept from 5 kHz to 80 kHz. Ferrite cores offer lower saturation flux density and low maximum hot spot temperature. Although, ferrites do provide lower core loss, the energy storage capability is the lowest compared to the others. In addition, the permeability and loss of ferrites are highly dependent on the temperature [33].

An unidirectional 1.2 kW CCM single-phase boost rectifier has been designed in [30] to compare the performance of two different core materials, ferrites and powder iron. Ferrites are preferred for inductors subject to a large current ripple. The fringing fields near the air gap impose an additional design constraint on the winding of the inductor. Powder iron cores also suffer from thermal aging problems, unless the core loss is limited to very low values.

Powder cores suffer less from thermal aging and hot spotting in the core compared to powder iron cores. MPP-Powder core has a better inductance independency to dc magnetization and the lowest core loss among other powder cores such as Kool-M$\mu$, High-Flux, and Mega-Flux [32]-[34]. However, MPP cores have lower saturation flux density compared to the other powder cores.

Amorphous shows a higher core loss than ferrite, despite offering higher saturation flux density compared to ferrite and Kool-M$\mu$. Like the Kool-M$\mu$ materials, amorphous also features a soft roll-off of the $B$-$H$ curve. This feature can be utilized to decrease the inductor volume by means of allowing the inductance to fall by a certain percentage at peak current [31]-[33].

In [33], it is concluded that the best trade-off between size and core loss is attainable using the amorphous core. The Sendust (such as Kool-M$\mu$) material can be adopted for high ripple conditions since the loss remains relatively constant despite increasing the ripple of magnetic field intensity. Moreover, the powder materials are good candidates for PWM filters, especially at high ripple currents. However, this paper has not considered the effect of power level on selecting the optimum material.

To summarize the literature review, TABLE 2-2 is listed the magnetic materials properties. Although, TABLE 2-2 gives a clear picture on what type of material can lead to lower core loss, the power level of the magnetic component can change the priorities. For instance,
TABLE 2-2: Comparison between magnetic core materials.

<table>
<thead>
<tr>
<th>Core type and manufacturer</th>
<th>Material</th>
<th>$B_{sat}$ (T)</th>
<th>Core loss density(W/mm³) $@0.1T$, 50 kHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Powder core- Magnetics [34]</td>
<td>MPP-60µ</td>
<td>0.7</td>
<td>$357.1 f^{1.412} B^{2.05} = 255$</td>
</tr>
<tr>
<td></td>
<td>KoolMj-60</td>
<td>1</td>
<td>$193 f^{1.29} B^{2.01} = 300$</td>
</tr>
<tr>
<td></td>
<td>High Flux</td>
<td>1.5</td>
<td>$492 f^{1.32} B^{2.22} = 518$</td>
</tr>
<tr>
<td>Ferrite- Ferroxcube [35]</td>
<td>3C92</td>
<td>0.46</td>
<td>60</td>
</tr>
<tr>
<td>Ferrite-TDK [36]</td>
<td>PE90</td>
<td>0.43</td>
<td>25</td>
</tr>
<tr>
<td>Amorphous-Hitachi Metals [37]</td>
<td>2605SA1</td>
<td>1.56</td>
<td>$46.7 f^{1.51} B^{1.74} = 313$</td>
</tr>
<tr>
<td>Powder iron- Micrometals [38]</td>
<td>Mix-26</td>
<td>1.38</td>
<td>1800</td>
</tr>
</tbody>
</table>

Ferrite cores offer the lowest core loss density but depending on the number of turns it may yield a larger copper loss. Or the core loss in ferrite core may drastically increase due to the dc magnetization effect depending on the current ripple and power level. In Chapter 3, an appropriate core material will be chosen to have a balance between the core and copper loss, therefore to achieve an optimum design for the inductor.

2.3. Filter design

This section is divided into the following categorizations:

i) *Filter parameter design including damping method* (i.e. passive and active damping):

Filter design has largely been investigated for grid-connected VSCs. The main objective of employing the filter is to fulfill the grid regulations (e.g. IEEE 519 [9] and [43]). Among numerous papers in this area [45]-[65], several papers that are mostly related to the PhD work have been selected and studied [45]-[50] in the following.

A general and step-by-step approach for designing LCL filter of grid-connected rectifiers has been introduced in [45]. Control design and the impact of employing LCL filter on controller and its performance are also discussed in this paper. The grid-side inductance value is chosen as a function of the converter-side inductor. However, choosing the converter-side inductance value is not explained. Another iteration based solution for designing LCL filter has been developed in [46]. A margin for the converter and grid side inductance values is presented according to the operation principle of the converter and the filter resonant is damped by an active method. Optimization of LCL filters with passive damping in terms of loss and size has been investigated in [48]-[51]. In [48] and [49], the damping branch is configured as shown in Fig. 2.1 and the damping resistor is designed to reduce the power losses and provide a proper damping. Different passive damping configurations are investigated in [50]. The tradeoff between the effectiveness, the simplicity, and the power dissipation of different -
damping configurations, the damping in this work will be as shown in Fig. 2.1. In TABLE 2-3, a summary of the presented papers is provided. The filter configuration with $R_dC_d$ passive damping is shown in Fig. 2.1. This table lists the calculated LCL filter parameters by the papers for specific converter parameters which will also be studied in this PhD work. The converter is a 5 kW three-phase VSC with 45 kHz switching frequency, 230 V line voltage, and 700 V dc link voltage.

In Chapter 3, an LCL filter will be designed for the converter with the mentioned specifications and will be compared with TABLE 2-3.

ii) Controller and Stability analysis:

After designing the filter, converter control stability by considering different grid conditions needs to be studied [45]-[55],[60],[61],[72]-[77]. The stability analysis has been categorized into two methods, impedance-base and passivity-based analysis [73]. According to these different methods, the stability of the controller for employing active or passive damping is also studied for different grid conditions in [61],[68],[76], and [77]. In this work, the controller stability is analyzed using the impedance based analysis. Moreover the intention for controller design in this work is not to improve the existing methods or suggest new approaches. It mainly focuses on using the most suitable method for analyzing the impact of different controllers on the conversion efficiency. Two controllers are used in this thesis, PI controller in the rotational reference frame and PR controller in the stationary reference frame. For design purpose, [45]-[46] for PI and [69] for PR are used.

2.4. Summary

The summary of the state of the art deduced from the literature search is as follows:

- The conversion efficiency of the most recent publications is studied and the specifications of each converter are collected. This provides a fair comparison between the current state of the art and this PhD research work.

- In many of the publications, comparisons between different core materials for different applications have been made. The impact of the power range on the optimum selection of these core materials for any specific application has to be considered.
According to the converter specifications in next chapter, using core characteristics give an appropriate core material.

- Most often, the designing methods of $LCL$ filters yield an oversized and the final method is based on iteration. The current and voltage behavior of the filter parameters based on the switching pattern of the converter has not been studied for identifying an optimum filter in terms of loss/size.

- Due to the effectiveness, simplicity and relatively low power dissipated in the damping of an $LCL$ with a resistive-capacitive damping branch, in Chapter 3 the same filter and damping will be used.

- Although the control of grid-connected converters is vastly studied in the literature, the impact of different controllers and their parameter settings on the overall efficiency of the converter has not been studied.
3. Two-Level Three-phase Power Factor Correction Rectifier

3.1. Introduction

In this chapter, two-level three-phase PWM voltage source converter (VSC) in power factor correction applications (PFCs) is thoroughly analyzed to achieve high conversion efficiency. After describing the system, step by step design of an \(LCL\) filter will be presented. The objectives for designing the filter parameters are:

- To optimize the required filter parameters to have relatively small and high efficient filter at operating switching frequency.
- To present a generalized model for filter design which can also be used for designing a filter for a three-level converter [see Appendix A].

By obtaining the required filter parameters which successfully fulfill the grid regulations (see section 3.2), the loss distribution in a silicon-carbide (SiC) based three-phase VSC will be analyzed.

3.2. System description

In Fig. 3.1, the schematic of a two-level three-phase power factor correction rectifier (PFC) is shown. The converter is a 5 kW SiC based two-level three-phase PWM PFC rectifier and its specifications are listed in TABLE 3-1. The grid regulations have directed the grid connected converters to provide a good current harmonic performance. Therefore, a high order filter such as \(LCL\) filter is required to fulfill the grid regulations. The harmonic current injection limit for grid-connected system where the rated voltage at point of common coupling (PCC) [see Fig. 3.1] is 120 V to 69 kV is recommended by IEEE 519 standard. These current harmonic limits are listed in TABLE 3-2.

The filter configuration shown in Fig. 3.1, consists of the converter-side inductor (\(L_c\)), the grid side inductor (\(L_f\)), and the filter shunt branch shown with \(Z_{Cf}\). All the inductances are shown with impedance, because the resistive behavior of the reactive components is also included in the analysis. The filter shunt branch can be replaced with different combination of passive elements.

TABLE 3-1: General system specifications and base values for per-unit system.

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P_{nom})</td>
<td>Nominal power (kW)</td>
<td>5</td>
</tr>
<tr>
<td>(V_{ac})</td>
<td>Phase source voltage- rms (V)</td>
<td>230</td>
</tr>
<tr>
<td>(V_{dc})</td>
<td>DC link voltage (V)</td>
<td>565-700</td>
</tr>
<tr>
<td>(f_g)</td>
<td>Grid frequency (Hz)</td>
<td>50</td>
</tr>
<tr>
<td>(Z_g)</td>
<td>Grid impedance ((\Omega))</td>
<td>(20%\times Z_{b}^1)</td>
</tr>
</tbody>
</table>

\(^1\)The maximum grid impedance has been calculated by maximum short circuit current at PCC using IEEE-519 standard.
### TABLE 3-2: Maximum current harmonic distortion in percentage of rated current according to IEEE519.

<table>
<thead>
<tr>
<th>Harmonic order</th>
<th>5</th>
<th>7</th>
<th>11</th>
<th>13</th>
<th>17</th>
<th>19</th>
<th>23≤h&lt;35</th>
<th>h ≥35</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_h/I_g ) (%)</td>
<td>4</td>
<td>4</td>
<td>2</td>
<td>2</td>
<td>1.5</td>
<td>1.5</td>
<td>0.6</td>
<td>0.3</td>
</tr>
</tbody>
</table>

* Even harmonics are limited to 25% of the odd harmonics. 
** \( I_g \): maximum grid current and \( I_h \): grid current harmonic.

### 3.3. Filter design

In this section, filter parameters will analytically be designed to achieve an optimum filter as well as a general method for designing filter.

For further analysis several assumptions have to be taken as follows:

1) The grid voltage is balance. Therefore, analysis is presented for only one phase (e.g. phase ‘a’);
2) The switching frequency is much higher than the grid frequency (i.e. \( f_{sw} \gg f_{grid} \));
3) The modulation scheme is sinusoidal pulse width modulation (SPWM);
4) The modulation is center-based pulse width modulation.

The equivalent single-phase circuit can be depicted as shown in Fig. 3.2. The filter voltage is found as follows:

\[
\text{\( v_{\text{filter}}(t) = v_{\text{PCC}}(t) - v_{an}(t) \)}
\]

(3.1)

where \( v_{\text{filter}} \) and \( v_{\text{PCC}} \) are the filter and PCC voltage, respectively. \( v_{an} \) can be expressed as a function of the common mode voltage (\( v_{nN} \)) and the ac link voltages.

\[
\text{\( v_{an}(t) = v_{aN}(t) - \frac{1}{3} v_{nN}(t) = \frac{2}{3} v_{aN}(t) - \frac{1}{3} v_{bN}(t) - \frac{1}{3} v_{cN}(t) \)}
\]

(3.2)

where \( v_{aN} \) is the ac link voltage of phase \( x \) (\( x = a, b, c \)).

---

**Fig. 3.1:** The schematic of a two-level three-phase PFC.
The fast Fourier transform (FFT) of the ac link voltage for “phase a” is derived based on the Bessel function for a naturally sampled SPWM (i and j are carrier and base-band index variable, respectively) and based on (3.2) the converter voltage FFT can be derived as follows [10]:

\[
v_{an} = V_{dc} m_a \cos(\omega_g t) + \frac{4V_{dc}}{\pi} \sum_{i=1}^{\infty} \sum_{j=-\infty}^{\infty} \frac{1}{i} J_n\left(i \frac{\pi}{2} m_a \right) \sin\left([i + j] \frac{\pi}{2}\right) Q(t)
\]  

(3.3)

where \(m_a\) is the modulation index, \(V_{dc}\) is the dc link voltage, \(\omega_g\) is the fundamental angular frequency, and \(Q(t)\) is as follows:

\[
Q(t) = \cos\left((i\omega_{sw} + j\omega_g) t\right) - \frac{1}{3} P(t)
\]  

(3.4)

\[
P(t) = \cos\left((i\omega_{sw} + j\omega_g) t\right) + \cos\left((i\omega_{sw} + j\omega_g) t - 2n\pi / 3\right) + \cos\left((i\omega_{sw} + j\omega_g) t + 2n\pi / 3\right)
\]  

(3.5)

\(\omega_{sw}\) is the switching or carrier angular frequency.

According to (3.3), it can be seen that the largest converter voltage harmonics happen at side-band of carrier frequency where \(j = \pm 2\) and \(i = 1\) and this voltage reduces at multiple of carrier frequency (i.e. \(i = 2, 3, \ldots\)). Therefore, the main concern for designing the filter is \(f_{sn} \pm 2f_{cs}\) [10].

### 3.3.1. Converter-side inductor

Since minimum required inductance value depends on modulation index, following analysis is divided into linear modulation and overmodulation.

#### 3.3.1.1. Linear modulation region

Generally, to fulfill the grid regulations, relying on converter-side inductor results to a bulky and expensive solution which is out of the objective of this project. Therefore, increasing the order of the filter could potentially reduce the overall size of the filter and accordingly losses. If filter is designed correctly, the voltage after the converter-side inductor is essentially sinusoidal and the amplitude is close to PCC voltage (very small voltage drop on \(L_f\)).

Therefore, it can be said that the converter-side inductor voltage is independent from the filter configuration and converter voltage (i.e. \(v_{an}\)) determines the minimum required inductance value [46]. Hence, the circuit shown in Fig. 3.1 can be simplified to Fig. 3.3(a) where \(v_C\) is the voltage across the shunt branch. Then, in (3.1) instead of filter voltage, inductor voltage
can be replaced and instead of $v_{PCC}$, $v_C$. Fig. 3.3(b) shows the inductor voltage and the resultant current which flows through the inductor. As this figure indicates, inductor voltage shows a repetitive pattern in each quarter of grid period. There are two time intervals that the inductor voltage has similar behavior. Since, $v_C$ is sinusoidal, it can be concluded that this pattern is generated by $v_{an}$.

The first interval is when the reference voltage of “phase $a$” is between the other phases (i.e. $0 < \omega t < \pi/3$). The next interval is when the reference voltage of “phase $a$” is larger than the other references (i.e. $\pi/3 < \omega t < \pi/2$). Using the general expression of inductor voltage, the average value of the current ripple can be found for region I and II. The detail procedure of deriving the average current is explained in Appendix B1 and Appendix B2.

$$v_{Lc}(t) = v_C(t) - v_{an}(t)$$  \hspace{2cm} (3.6)

$$\Delta i(t) = \frac{v_C(t) - v_{an}(t)}{L} \Delta t$$  \hspace{2cm} (3.7)

This observation also illustrates that in each time interval, there is a maximum current ripple. For the first time interval, the maximum current ripple happens at zero crossing (i.e. $\omega t = 0$). The reference voltage of phase $a$, $b$, and $c$ are 0, $m_a V_m \sin(-2\pi/3)$, and $m_a V_m \sin(2\pi/3)$, respectively. The maximum current ripple for the second interval happens at peak current (i.e. $\omega t = \pi/2$). Reference voltage of phase $a$ is $m_a V_m$ and for phase $b$ and $c$ are $-m_a V_m \sin(\pi/6)$.

![Diagram of Three-Phase Grid-Connected Voltage Source Converter](image)

Fig. 3.3: (a) Simplified schematic of three-phase grid-connected voltage source converter, (b) the inductor current and voltage waveforms.
As a result, maximum current ripple in each interval is calculated as follows:

\[ L_c = \frac{\sqrt{3}}{12} \frac{V_{dc}}{f_{sw} \Delta i} m_a \theta = k \pi, \ k \in \{0, 1, 2, ...\} \]  

(3.8)

\[ L_c = \frac{V_m}{2 f_{sw} \Delta i} \left(1 - \frac{m_a}{2}\right) \theta = \left(2k + 1\right) \frac{\pi}{2}, \ k \in \{0, 1, 2, ...\} \]  

(3.9)

Maximum current ripple occurs at peak of the current when (3.10) is correct.

\[ \frac{V_{dc}}{V_m} \leq \sqrt{3} \left(\frac{2}{m_a} - 1\right) \]  

(3.10)

By simplifying (3.10), the maximum current ripple happens at peak of the current when \(m_a \leq 0.845\). The complete procedure of calculating the current ripple for this system is explained in Appendix B1 and Appendix B2.

### 3.3.1.2 Overmodulation

The analysis provided in the previous section is focused on the linear modulation of SPWM. Reducing dc link voltage is beneficial for both reducing the inductance value and therefore reducing size of the filter and also reducing the switching loss. As it is seen from (3.8) and (3.9), the inductance value is directly a function of dc link voltage. There are different methods that expand the linearity of the modulation such as third harmonic injection PWM (THPWM) and space vector PWM (SVPWM). Here, the current ripple at zero crossing and peak current for THPWM is studied. The details of current ripple determination for THPWM are fully explained in Appendix B1.

Similar to the analysis for linear modulation, the current ripple at zero crossing and peak of the current are analyzed which is shown in Fig. 3.5(a) and (b), respectively.
Fig. 3.5: The current ripple for THPWM (a) at zero crossing \( (m_a = 2/\sqrt{3}) \) and (b) at peak of the current.

According to the current ripple waveform shown in Fig. 3.5(a), the inductance value for maximum modulation index in THPWM \( (m_a = 2/\sqrt{3}) \) is found as:

\[
L_c = \frac{V_{dc}}{6 f_{sw} \Delta i} \tag{3.11}
\]

Interesting point that can be drawn from (3.11) is that if in (3.8) instead of modulation index the maximum modulation index in THPWM or SVM is replaced (i.e. \( m_a = 2/\sqrt{3} \)) then (3.11) is obtained. Therefore, it can be concluded that (3.8) is a general equation for current ripple at zero crossing of a two-level three-phase PFC using continues PWM such as SPWM, THPWM or SVM.

The same procedure can be done for the peak current and its current ripple for THPWM as following. To utilize the most of dc link \( m_3 \) (which represents the modulation index for the third harmonic) should be equal to one-sixth of modulation index and to have low switching loss \( m_3 \) is set to one-fourth of modulation index [10] and [78]-[80]. Therefore, to have a general expression for current ripple at peak current the term \( m_3 \) will be kept as it is. Fig. 3.5(b) shows the current ripple at peak current in one switching cycle.

By referring to Appendix B1, the current ripple for the peak current in THPWM is obtained as follows:

\[
\Delta i = \frac{\sqrt{3} V_{dc}}{6 L_c f_{sw}} m_a \left( 1 - \frac{m_a}{2} - m_3 \right) \tag{3.12}
\]
Unlike (3.11) which is not dependent on the modulation index, (3.12) is a function of modulation index. Moreover, comparing (3.11) and (3.12) demonstrates that the current ripple at peak current for overmodulation is smaller than zero-crossing current ripple. This confirms that since in overmodulation $m_a$ is larger than 0.845 then certainly the current ripple at zero crossing is dominant.

### 3.3.1.3. Three-wire PFC and four-wire PFC

In line with the main objective of the project, the impact of connecting dc link midpoint to star point of the filter on boost inductor size and converter efficiency is studied and presented in Appendix B3. The conclusion of this comparison can be summarized as follows:

- Inductance value for the four-wire PFC is larger than the one for three-wire PFC.
- Maximum current ripple in three-wire PFC depends on modulation index for linear modulation while in four-wire is not a function of modulation index.
- Current harmonic behavior of four-wire PFC is similar to the single phase PFC in which the main harmonics happens at switching frequency.
- Minor $B-H$ loops generated by the current ripple in inductors in both converters are different and in four-wire it is easier to generalize the high frequency core losses. More details on core loss calculation of four-wire PFC have been mentioned in Appendix B8.
- The overall efficiency of the three-wire converter is higher than four-wire converter with an identical current ripple limit.

### 3.3.2. Filter capacitor

Position of the current and voltage sensors in grid-connected voltage source converters can affect the power factor and the control. Converter synchronizes itself with grid voltage, so voltage sensor must be positioned on grid side [53]. However, current sensor can be positioned either at grid side or converter side [53]. If the current sensor is positioned at the grid side then the outcome of controller is a voltage and current in phase. On the other hand, power factor cannot be one when current sensor position is at the converter side. But this configuration provides a good fault protection for the converter. Besides, in controller which will be explained later, the phase shift between grid voltage and current can be compensated [12]. Fig. 3.6 shows single-phase diagram of an $LCL$ filter for both sensors positions along with their vector diagram. In the first case, the converter is seen as a capacitive load for grid and in the second sensors position, it is pure resistive. For this PhD work, the sensors are positioned as shown in Fig. 3.6(a).

The phase difference between $I_g$ and $V_{PCC}$ can be achieved as follows (in steady-state condition, $f_g = 50$ Hz):

$$ I_g = I \left( \frac{1}{1 - C_f L_f \omega_g^2} \right) + jV_{PCC} \left( \frac{C_f \omega_g}{1 - C_f L_f \omega_g^2} \right) $$

(3.13)
Fig. 3.6: The position of the sensors- single phase equivalent circuit of LCL filter (a) voltage sensor at PCC, current sensor at converter-side (b) voltage and current sensor at PCC, (c) the vector diagram of first sensor position and (d) the vector diagram of second sensor position.

\[ \theta_{\text{current}} = \tan^{-1}\left( C_f \omega_s \frac{V_{\text{PCC}}}{I} \right) \]  

(3.14)

This phase difference can be compensated using the control system, however as it is mentioned in the literature the limit for the absorbed reactive power by filter capacitor is considered 5% of apparent power [45].

\[ \omega_s Z_b C_{f, \text{max}} = 0.05, \quad Z_b = V_b^2 / S \]  

(3.15)

where \( Z_b \), \( V_b \), and \( S \) are the base impedance, voltage and apparent power, respectively.

For capacitor lower limit, high frequency current ripple which flows through the filter capacitor needs to be calculated to define the minimum required filter capacitor. Ideally, the current ripple flows through the filter capacitor. Therefore, the maximum converter current ripple determines the minimum required capacitance value. The minimum required filter capacitor can be obtained by (3.16) for peak current.

\[ C_{f, \text{min}} = \frac{V_m}{32 L_c f_{sw}^2 \Delta V_{\text{ripple}}} (1 + m_a)(1 - m_c / 2) \]  

(3.16)

In (3.16), \( L_c \) is replaced by (9), then (3.16) becomes as follows:

\[ C_{f, \text{min}} = \frac{\Delta i}{16 f_{sw} V_{\text{ripple}}} \left( 1 + m_a \right) \]  

(3.17)

Normally, current ripple is considered between 10-30% of nominal current and voltage ripple is considered lower than 5% of nominal ac voltage. Replacing these values (\( k_1 \) for current
ripple and \( k_2 \) for voltage ripple, respectively) in (3.17) and normalized it with respect to \( C_{f,\text{max}} \) then the following equation presents the normalized minimum required filter capacitor.

\[
C_{f,\min} = \frac{k_1}{16k_2} \frac{(1 + m_0)}{f_{sw}} \omega \bar{C}_{f,\text{max}}
\]  

(3.18)

From (3.18) it can be concluded that minimum required inductance is a function of switching frequency and modulation index. The derivation method in details is presented in Appendix B4 and Appendix B5.

3.3.3. Damping

From Fig. 3.2, the admittance from converter side point of view is obtained as follows:

\[
Y_{eq} = \frac{i(s)}{v_m(s)} = \frac{1}{\left( (Z_{l_f} + Z_{r_f}) \| Z_{c_f} \right) + Z_{l_i}}
\]  

(3.19)

Although putting a resistor in series with filter capacitor is completely against the objective of the project, damping provided by the resistor can be extended by minor changes for other shunt configurations [45],[50], and [57]. To simplify, the admittance can be written for a simple damping resistor \( R_d \) in series with capacitor \( C_d \) as a function of the filter parameters (the resistive elements of reactive components are neglected) [see Fig. 3.7(a)].

\[
Y_{eq} = \frac{\left( L_i + L_y \right) C_s s^2 + R_c C_s + 1}{L_c (L_i + L_y) C_s s^3 + R_c C_d (L_i + L_j + L_y) s^2 + (L_i + L_j + L_y) s}
\]  

(3.20)

The root-locus breakaway point of the transfer function when \( R_d \) is assumed to be a gain can give the maximum damping resistance [see Fig. 3.7(b)]. The higher limit of damping resistance can be found by calculating the breakaway point of root-locus as follows:

\[
R_{d,\text{max}} = \frac{2}{C_d} \sqrt{\frac{L_c \left( L_i + L_j \right) C_d}{L_c + L_y + L_j}} = \frac{2}{C_d \omega_n}
\]  

(3.21)

And the lower limit is found when \( \zeta = \sqrt{2}/2 \) as follows:

\[
R_{d,\text{min}} = \sqrt{\frac{2L_c \left( L_i + L_j \right)}{(L_c + L_y + L_j) C_d}}
\]  

(3.22)

To reduce the power loss in the damping branch, filter capacitor \( C_f \) will be paralleled with \( R_d C_d \) which is shown in Fig. 3.7(c). Root-locus analysis shows increasing the filter capacitor needs more damping resistor to damp the resonance which leads to higher loss. But the attenuation after resonance frequency gets better.

Increasing the damping capacitor (\( C_d \)) leads to have more stable system and better transient response with lower damping resistor. But attenuation after resonance frequency reduces. As-
### CHAPTER III - TWO-LEVEL THREE-PHASE PFC

Three scenarios \((C_f + C_d = \text{cte})\):
1) \(C_f = 4C_d\), 2) \(C_f = C_d\), 3) \(C_f = 1/4C_d\)

---

**Fig. 3.7:** (a) LCL filter with resistive damping, (b) the corresponding root-locus for finding an optimum damping resistor, (c) LCL filter with RC damping, (d) the corresponding root-locus for three different scenarios where 1) \(C_f = 4C_d\), 2) \(C_f = C_d\), 3) \(C_f = 1/4C_d\) (in all scenarios \(C_f + C_d\) is kept constant).

It is concluded in literature review as well ([47], [48], [50], and [57]), the best configuration is to keep both filter and damping capacitors equal even though it brings more losses compared to the scenario where \(C_d\) is larger than \(C_f\).

Power loss in the damping branch can be calculated using FFT of the current in the damping branch. Calculation of loss in damping branch for both cases has been addressed in [57].

### 3.3.4. Grid-side inductor

Two methods are derived for calculating required grid-side filter inductance value.

#### 3.3.4.1. LCL with resistive damping

The first method is using the filter configuration shown in Fig. 3.7(a). The capacitor ideally draws all the high frequency current harmonics. If the damping resistor is correctly chosen, the impedance of the damping branch is still smaller than the impedance of the grid-side filter inductance at switching side-band frequency [Fig. 3.7(a)]. By adding the damping resistor, the grid-side filter inductor voltage is influenced by the current ripple flowing through the
filter capacitor. As it can be seen in Fig. 3.8(a), the current which flows through the damping branch is forming the voltage across it and causes that the voltage across the grid inductor is also affected by the damping branch. On the other hand, the converter current shows its effect on the grid-side inductor voltage. Fig. 3.8(b) shows the grid current and filter inductor voltage in one switching cycle at peak current. The aim is to present maximum current ripple for this inductor as shown with $\Delta i_{g,max}$ as a function of damping resistor.

The minimum required grid filter inductance value, then, is derived as a function of the damping resistor and the converter current ripple as follows:

$$L_{f,min} \approx R_d \frac{\Delta i_{max}}{18 f_{sw} \Delta i_g} (1 + m_a)$$  \hspace{1cm} \text{(3.23)}

where $\Delta i_g$ is the maximum allowable current ripple at grid side with respect to the grid regulations. Using (3.22) and (3.23), the values for $L_f$ and $R_d$ can be calculated. The complete method of deriving the inductance value for the grid filter has been conducted in Appendix B1 and Appendix B5.

### 3.3.4.2. LCL filter design with LISN

Designing filter parameters often ends up with oversizing, since the design is for a stiff grid or literally for no grid impedance. Therefore, the overall loss in filter increases in despite of this fact that the grid impedance is constantly changing. Providing well-defined grid impedance which is defined by the standards for choosing filter parameters can be beneficial for having an optimum filter and providing repeatable measurements. By introducing the WBG switches, the capability of having high frequency converter has increased which means the major converter current harmonics drops at high frequency where Line impedance stabilizing network (LISN) can provide well-defined impedance.

As it was mentioned in Section 3.3.1, the major PFC current harmonics happens at side-band
of switching frequency. Besides, using SiC switches has increased the switching frequency and then the side-band harmonics will certainly drop in the region that LISN can actively provide constant impedance. The equivalent circuit of the filter with LISN is shown in Fig. 3.9.

The converter-side inductor and the filter capacitor are derived in the previous sections using (3.8), (3.18), and (3.22), respectively. To optimally design the grid side filter inductance, the equivalent circuit is used and the required inductance value to fulfill the grid regulation is achieved as follows:

\[
L_f = \left( \frac{V_\text{an}}{I_\delta} \right)^2 \left[ (R_{\text{LISN}} \alpha)^2 - L_c \omega_h \right] \frac{1}{\alpha \omega_h}
\]

\[
\alpha = C_f L_c \omega_h^2 - 1
\]

Deriving of (3.24) is explained in details in Appendix B4.

The value of the grid-side inductor using the first method of damping is three times bigger than the second damping method. In next section where the loss distribution will be studied, the loss different between these two methods will be also discussed.

3.3.5. Filter comparison

Two different \(LCL\) filter has been designed and results are listed in TABLE 3-3 for a 5 kW SiC based three-phase PFC with 45 kHz switching frequency [see Fig. 3.7(a)&(c)] (the reason on selecting 45 kHz as switching frequency is explained in Section 3.7). The converter-side inductance is independent from the filter configurations, hence using (3.8) for 30% current ripple gives the minimum converter-side inductance for the higher dc link voltage (i.e. 700 V, see TABLE 3-1). Eq. (3.23) and (3.24) are used for determining the grid-side filter inductance for both filter configurations, respectively. Using damping branch in parallel with filter capacitor reduces size of the grid-side filter inductance to 1/3. According to (3.15) and (3.18), the margin regardless of the filter configuration for minimum and maximum filter capacitor is determined which is 2.5 \(\mu\)F and 5 \(\mu\)F, respectively. Based on the lower margin defined in (3.22), the damping resistor for \(LCL\) with \(R_d\) is calculated. The damping resistor for \(LCL\) with \(R_dC_d\) is also determined using root-locus analysis-scenario 2-shown in Fig. 3.7(d). TABLE 3-3 is the summary of designed filter for both configurations.
According to the parameters, the second design will lead to higher efficiency and therefore it will be used for the final converter design.

### 3.4. Layout design

Different layouts have been designed in this project and finally the optimum layout has been taken which lead to higher conversion efficiency. The driver voltage for turn on and off has been kept +15 V for turning on and -5 V for turning off [81]. In the beginning of the project, the driver from Cree was used [82]. However, to place the driver as close as possible to the switches for reducing the gate inductance, the driver layout changed.

The drive layout is also modified to provide proper shielding to the gate driver circuit to avoid any noise injection at the gate of SiC MOSFETs. The parasitic inductance in the whole converter is reduced as much as possible to avoid any voltage spikes for the SiC MOSFETs. Although, SiC MOSFET switches have relatively low charges compared to alternative Si MOSFET, the fast transient current during each switching instant can cause ringing in the circuit. In order to reduce the parasitic inductance, ground and power planes or traces as well as the decoupling capacitors are placed as close as possible to switches. In half bridge configuration, the connection between the top and bottom switches (i.e., high side and low side switches) is maintained very short by keeping them back to back on the PCB. Modular design has been constructed in this layout to make sure the conditions for all phases are identical.

The positive and negative dc rails are placed on top of each other to confine the field in a very small area. In addition, since the plates are wide and short the ac resistance of the plate is reduced. The loop is also small and the parasitic inductance of each plate is also reduced.

The efficiency has increased by introducing the new layout. The efficiency curve which has been shown in Appendix B3, results in the peak efficiency of 98.6%. In the new design, the layout and inductors have been modified to achieve the peak efficiency of 98.95% which will be explained in Chapter 4.

### 3.5. DC link capacitor

DC link capacitance value has been calculated according to the presented method in [85]. The dc link capacitor is facing high frequency voltage ripple coming from switching pattern and its value can be affected by the modulation scheme [85]-[86]. Furthermore, the capacitance
has to be sufficient to keep the dc link voltage constant during the transient. Because, the delay introduced in signal measurements can cause noticeable transient for the dc link voltage.

The minimum filter capacitance for 5% voltage ripple and voltage measurement delay time of 1 msec is 100 μF. To reduce the ESR of the dc link capacitor, Film capacitor has been used and 6 of them are paralleled. To provide middle point connection for the dc link two electrolytic capacitors are added in parallel with two film capacitors. The final dc link capacitance value is 144 μF. The dc link capacitor configuration is shown in Fig. 3.10.

3.6. Loss distribution

In this section, loss distribution in two-level three-phase PFC will be explained. Core loss and copper loss in filter inductors and damping power loss in damping branch will be calculated. The conduction loss after determining the converter-side inductor is also explained and finally the switching loss is achieved.

3.6.1. Inductor loss

According to the literature review and TABLE 2-2, although MPP core has lower saturation flux density compared to other powder cores, it offers lower core loss. In addition, the effect of dc magnetization on core loss is very small in this type of core. Therefore, MPP core has been utilized for design of high frequency inductor in this work (i.e. \( L_c \)). During the process of design, a great attention has been dedicated to the saturation flux density, size and number of winding turns to avoid saturation and increasing the ac copper resistance. The specifications of the inductor are shown Fig. 3.11(a).

Due to the effect of dc magnetization (i.e. change in permeability), the inductance value changes by the fundamental grid frequency current as it is shown in Fig. 3.11(b) for different load conditions. As it can be seen, no-load inductance value is 870 μH and when the current is lower than 2 A the inductance value will be the same. As soon as the instantaneous current increases more than 2 A, the inductance value starts to decrease. The full load inductance is
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3.6.2 Switching loss

Device capacitance (i.e. $C_{GS}$, $C_{GD}$, and $C_{DS}$) plays an important role in determining the energy loss during each switching transition. The required charge at turn-on and turn-off state determines the capacitance losses in switches. Due to the non-linearity of the gate-drain capacitor, the output capacitor ($C_{OSS} = C_{DS} + C_{GD}$) is also nonlinear.

To calculate the capacitive switching loss, the output charge must be calculated. In device datasheet, normally the output charge has given for a specific test condition and drain-source voltage which might be different from the test condition of the converter. Therefore, this value needs to be calculated for the operating voltage of the converter as in (3.25).
TABLE 3-4: Comparison between SiC and Si MOSFETs (1200 V, 30 A).

<table>
<thead>
<tr>
<th></th>
<th>SiC MOSFET [89]</th>
<th>Si MOSFET [90]</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{DS(ON)}$</td>
<td>80mΩ</td>
<td>350 mΩ</td>
</tr>
<tr>
<td>$C_{iss}$ (pF)</td>
<td>525</td>
<td>22500</td>
</tr>
<tr>
<td>$C_{oss}$ (pF)</td>
<td>134</td>
<td>950</td>
</tr>
<tr>
<td>$Q_g$ (nC)</td>
<td>49.2*</td>
<td>310**</td>
</tr>
</tbody>
</table>

$V_{ds} = 800$ V, $I_D = 20$ A, $V_{drive} = 0/20$ V.
$V_{ds} = 800$ V, $I_D = 12.5$ A, $V_{drive} = 0/10$ V.

\[
Q_{oss} = \int_{0}^{V} C_{oss}(v) \, dv
\]  
(3.25)

where, $V$ is the drain-source voltage (i.e. for this converter is dc link voltage) and $C_{oss}(v)$ is the variant output capacitance of the device with instantaneous drain-source voltage. By modifying the output charge of the switch, capacitive loss can be calculated as follows:

\[
P_{cap.} = \frac{1}{2} Q_{oss} V_{ds} f_{sw}
\]  
(3.26)

In addition to capacitive loss, turn-on and turn-off loss during the transition also compose part of the loss in the whole converter. However, due to the fast switching transient of current and voltage of SiC devices, the loss due to the capacitive loss is larger than this transition.

\[
P_{sw} = \frac{1}{2} V_{ds} f_{sw} \left[ (t_{on} + t_{off}) + (t_{on} + t_{off}) \right]
\]  
(3.27)

Another loss which contributes to the switching loss is drive loss. SiC devices have very low gate drive losses due to the small input capacitance ($C_{iss}$). The comparison between two switches one SiC and other Si MOSFET shows the difference between the characteristics in TABLE 3-4. Drive loss in the device is given as follows:

\[
P_{drive} = V_{drive} f_{sw} Q_G
\]  
(3.28)

where, $V_d$ is the gate drive reference voltage, $f_{sw}$ is the switching frequency and $Q_G$ is the total gate charge.

The other loss in switch is the conduction loss which is calculated as follows:

\[
P_{cond} = R_{DS} I_D^2
\]  
(3.29)

Therefore, the power dissipation due to the switching is $P_{sw} + P_{cap} + P_{drive} + P_{cond}$, all these parameters except conduction loss are a function of switching frequency. Therefore, the critical switching frequency can be achieved when the independent loss from switching is equal to the rest of the switching loss.
3.7. Selection of switching frequency

Although having high frequency converter leads to smaller magnets, switching loss can be the bottle neck of loss distribution in the converter. The losses in the converter components are all dependent on the switching frequency. In order to find a tradeoff between size and efficiency, a comparison has been conducted for three different switching frequencies:

1) 25 kHz,
2) 50 kHz, and
3) 75 kHz.

For any of these frequencies, the converter-side inductor is designed to keep the current ripple at 30% and therefore, the rest of the filter is not changed. The specifications of the designed inductor for each switching frequency are listed in TABLE 3-5. The material is MPP for all the inductors. The core loss is increased by reducing the frequency because of higher magneto motive force ($mmf$) which comes from higher number of turns (i.e. when $f_{sw} = 25$ kHz).

Since the current ripple is kept constant in all cases, the conduction loss in all three cases will be identical. However, the capacitive switching loss will be increased by frequency as explained in Section 3.6.2. To have an idea on how parameters are affecting each other and how the converter size and efficiency could be optimized Fig. 3.12 is depicted for three frequencies. Note that all the calculations are done at full power. As it can be seen, the lower frequency leads to have higher copper and core loss plus occupying more volume (more than 50% of all loss in the green area). On the contrary, higher switching frequency deviates the red area from core and copper loss toward switching loss.

Therefore, 50 kHz switching is an optimum tradeoff between the size, switching loss, core loss, and copper losses (see blue area in Fig. 3.12). In this work, the switching frequency is selected to be 45 kHz to keep the third multiple of switching current harmonics lower than the frequency where EMI standard is applying (i.e. 150 kHz). In next chapter, the measured efficiency will be shown and the results will be discussed in details.

3.8. Conversion efficiency

Loss distribution for the designed converter with the specifications stated in TABLE 3-6 is calculated and shown in Fig. 3.13 for different loads. As it can be seen, at full load the largest losses are allocated to loss in the switches (about 60%) and then inductor copper loss (about 25%). As soon as the power goes down the importance of idle losses such as capacitive loss, drive loss gets higher. For instance at 25% load, the idle loss contributes to more than 75% of total losses as it can be seen in Fig. 3.13.
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TABLE 3-5: Designed inductor for 25 kHz, 50 kHz, and 75 kHz.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>$L_c$ (mH)</th>
<th>Core material</th>
<th>Number of turns</th>
<th>Core loss (W)*</th>
<th>Copper loss (W)*</th>
</tr>
</thead>
<tbody>
<tr>
<td>25 kHz</td>
<td>1.16</td>
<td>MPP-C055617</td>
<td>115</td>
<td>1.32</td>
<td>6.86</td>
</tr>
<tr>
<td>50 kHz</td>
<td>0.580</td>
<td>MPP-C055439</td>
<td>82</td>
<td>0.85</td>
<td>3.65</td>
</tr>
<tr>
<td>75 kHz</td>
<td>0.386</td>
<td>MPP-C055439</td>
<td>60</td>
<td>0.77</td>
<td>2.7</td>
</tr>
</tbody>
</table>

*The core and copper loss at full load are written.

Fig. 3.12: The loss distribution in the converter at full load for three difference frequencies.

The best balance between the losses in the converter has happened at full load. The conduction loss, switching loss, and copper loss of the main inductor are dominant and equal to each other; while at half load the dominant power loss belongs to the switching capacitive loss. The SiC Schottky diodes can be used antiparallel with the SiC MOSFETs. These diodes have better performance with respect to the reverse recovery losses compared to the body diode of the SiC MOSFETs. However, the drop voltage across these diodes is higher in higher current than the drop voltage of the SiC MOSFET body diode. More importantly, adding these diodes causes an increase in the output capacitor of the switch which contributes in switching loss. In next chapter, a comparison of the measured efficiency will be presented by using SiC Schottky diode and not using them. The specifications of these diodes are listed in TABLE 3-6 as well.
### TABLE 3-6: Specifications of the components used in the converter.

<table>
<thead>
<tr>
<th>Component</th>
<th>Number</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power MOSFET</td>
<td>6</td>
<td>SiC C2M0080120D [89]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{d(60)} = 92 \text{ m\Omega}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Q_{on} @ 570V = 93.72 \text{ nC}$</td>
</tr>
<tr>
<td>Anti-Parallel Schottky diode</td>
<td>6</td>
<td>SiC C4D15120A [91]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$Q_c @ 570 \text{ V} = 68 \text{ nC}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_f @ 15 \text{ A and } 50^\circ\text{C} = 1.6 \text{ V}$</td>
</tr>
<tr>
<td>Converter-side inductor</td>
<td>3</td>
<td>Core MPP- C055439A2 [92]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$L_c : 580 \text{ \mu H}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Number of turns: 82</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Number of layers: 1 outer layer and 1.5 inner layer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Wire diameter: 1.42 mm</td>
</tr>
<tr>
<td>Filter capacitor</td>
<td>3</td>
<td>Metallized Polypropylene Film Capacitors-B32794</td>
</tr>
<tr>
<td>Damping capacitor</td>
<td>3</td>
<td>$C_f : 2.5 \text{ \mu F : } C_d$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ESR : 14 m\Omega @ 10 kHz</td>
</tr>
<tr>
<td>Grid-side inductor</td>
<td>3</td>
<td>Core MPP- C055439A2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$L_f : 100 \text{ \mu H}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Number of turns: 32</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Number of layers: 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Wire diameter: 1.5</td>
</tr>
<tr>
<td>Damping resistor</td>
<td>3</td>
<td>$R_d : 10 \text{ \Omega}$</td>
</tr>
</tbody>
</table>

![Loss distribution](image.png)

Fig. 3.13: The loss distribution in 5 kW SiC based three-phase PFC based on different load.

### 3.9. Summary

In this chapter, the converter current and voltage of the three-phase PFC have been analyzed. The following is a list of some of the conclusions and summary that can be drawn from the analyses presented in this chapter:

- The maximum current ripple for converter-side inductor depending on dc link voltage level can happen either at zero crossing or peak current.
If modulation index is higher than 0.845, then the maximum current ripple happens at zero crossing.

The derived equation for current ripple-(3.8)- can be used for sinusoidal pulse width modulation (SPWM) and third harmonic PWM.

The minimum filter capacitor is determined by current ripple introduced by the converter-side inductor.

It is shown that even at low switching frequency (e.g. 10 kHz) the filter capacitor by this method is achieved about half of the maximum filter capacitor. Therefore, a valuable margin is presented for the filter capacitor.

The optimum damping resistor for \textit{LCL} filter with RC damping branch increases when the filter capacitor increases (i.e. damping capacitor reduces).

Using line stabilization network (LISN) for designing the grid-side filter inductance leads to an optimum filter in terms of size and loss.

Using LISN for high frequency converters provides repeatable measurements for designing and testing the designed \textit{LCL} filter.

MPP core materials among other materials such as Ferrite, Amorphous, Kool-Mμ, High Flux offers smaller core loss and presents lower dependency on dc pre-magnetization for the power range of 5 kW. Special consideration must be taken to avoid saturation in MPP cores.

For a 5 kW three-phase PFC, the ac copper loss is negligible compared to the dc copper loss. Therefore, the solid round wire is the best option for winding the converter-side inductor.

The distribution of the losses between switches and the filter is optimum around 50 kHz switching for a 5 kW SiC based three-phase PFC.
4. Control of Three-phase Power Factor Correction Rectifier

This section focuses on the controller of the power factor correction rectifier and the influence of the controller choice on the conversion efficiency. Two types of current controllers will be studied 1) PI current controller in the rotational $dq$ reference frame and 2) proportional resonant (PR) controller in the stationary $\alpha\beta$ reference frame. The reason why two controllers have been studied in this work will be explained shortly.

Due to the nonlinearities of the converter such as the blanking time effect, the power quality decreases, especially at low power level. Using the $dq$ control without any harmonic compensation has been found to require an increase in the value of the converter-side inductance. In the previous chapter, the converter-side inductor was designed to have maximum current ripple of 30%. However, this causes a serious reduction in power quality. Therefore, the maximum allowed current ripple has been reduced to 15% to achieve an acceptable harmonic performance at low frequencies ($5^{th}$, $7^{th}$, $11^{th}$, $13^{th}$). This clearly changes the power loss distribution in the converter.

On the contrary, the simplicity of employing a harmonic compensator (HC) in a PR controller allows the maximum primary current ripple to be increased again to 30% while achieving the same harmonic performance.

Here the impact of the current controller on the efficiency can be seen. In addition, having better harmonic performance helps increasing the efficiency at low power which will also be discussed in this chapter.

4.1. System description

The general schematic of the setup is shown in Fig. 4.1. The current controller is either the PI or PR controller in the appropriate reference frame. The system consists of a three-phase SiC based PFC connected via an $LCL$ filter to the grid with passive damping. The $LCL$ filter contains a converter-side inductor ($L_c$), a grid-side inductor ($L_g$), a filter capacitor ($C_f$), and a damping branch comprising a capacitor $C_d$ in series with a damping resistor $R_d$. These filter parameters have been designed in Chapter 3.

The purpose of employing the controller is to keep the dc link voltage constant, program the current and power factor. The dc link voltage is controlled with an outer voltage loop and the output is the reference current for the inner current loop. The control system consists of a dc link voltage control loop with controller transfer function, $G_{c,dc}(s)$, and a current control loop with controller transfer function $G_c(s)$. The design of the current control loop for the $dq$ and $\alpha\beta$ control will be studied along with stability analyses. The dc link voltage control loop will be the same for both current controllers and will be studied subsequently.

4.2. Current controller

The current control loop is responsible for power quality and current protection. The block diagram of the closed-loop system with $G_c(s)$ as current controller is shown in Fig. 4.2(a). For
improving the performance of the controller, the voltage at the point of common coupling ($v_{PCC}$) is usually used [66]. In this case, $v_{PCC}$ is added with a gain denoted as $g_{cc}$.

The open loop transfer function of the system is then:

$$G_{OL}(s) = G_i(s)G_d(s)Y_{eq}(s)$$  \hspace{1cm} (4.1)

where $Y_{eq}(s)$ is the admittance of the $LCL$ filter along with the grid impedance seen from the converter side [see Fig. 3.2]. $G_d(s)$ is the transfer function of the pure time delay, $\lambda$, introduced by the PWM, ADC conversions, and the computation. Thus

$$G_d(s) = e^{-\lambda T_s s}$$  \hspace{1cm} (4.2)

For realization of the feedforward, the block diagram in Fig. 4.2(a) has changed to Fig. 4.2(b). This change is done for simplifying the further analysis. PCC voltage is added to the output of the current controller with a gain of $g_{cc}$ which can be set from 0 to 1. The open loop transfer function of the system with feedforward compensation is as follows:

$$G_{OLFF}(s) = \frac{G_i(s)Y_{eq}(s)G_d(s)}{1-g_{cc}G(s)G_d(s)} = \frac{G_{OL}(s)}{1-g_{cc}G(s)G_d(s)}$$  \hspace{1cm} (4.3)

where $G(s)$ is:

$$G(s) = g_{cc}Z(s)Y_{eq}(s)$$

$$Z(s) = \frac{v_{PCC}(s)}{i(s)} = \frac{Z_{L_{grid}}}{Z_C + Z_{L_{grid}} + Z_{L_{grid}}}$$  \hspace{1cm} (4.4)

According to the conclusion made in Appendix B6, feeding the PCC voltage as a feedforward to the current control loop helps reducing the sensitivity of the controller to the grid impedance. This improves the transient response of the current controller.
Fig. 4.2: (a) The block diagram of the PFC current control and (b) realization of feedforward effect as a block diagram for further analysis.

4.2.1. PI current control in the dq reference frame

To eliminate any steady state error in the current control with a constant current reference, the synchronous rotational reference or dq reference frame has been used. To control the power factor, the q-axis current component must be controlled. Due to the presence of the filter capacitor as it was mentioned in Section 3.3.2, the equivalent circuit from grid point of view is capacitive.

To compensate for the reactive power absorbed by the filter capacitor, the q-axis reference current cannot be set to zero. For designing this controller, the presented methods in [45],[46],[53], and [66]-[68] are used. It should be noted that the purpose of this section is not to introducing a new dq frame based control technique but to determine the conversion efficiency using an already established controller.

The current in d-axis is controlled by the dc link voltage control loop. The schematic of the controller has been shown in Fig. 4.3(a). The implementation of the PI current control loop is also shown in Fig. 4.3(b).

Since the filter capacitor only deals with the switching frequency ripple, the influence of it is neglected on the current controller [12], [45]. The LCL filter model and L filter model are practically the same for frequency larger than half of the filter resonant frequency. Therefore,
Fig. 4.3: (a) the block diagram of the controller in the dq reference frame and (b) the block diagram of the PI current controller.

The equivalent circuit shown in Fig. 3.2 can be simplified to Fig. 4.4. Accordingly, the grid current can be written as follows:

\[ R_T i_g + L_T \frac{di_g}{dt} = v_{\text{PCC}}(t) - v_{an}(t) \]  \hspace{1cm} (4.5)

where \( R_T = R_g + R_f + R_c \) and \( L_T = L_g + L_f + L_c \). Analyzing the system in the synchronous rotating reference frame, (4.5) will be written in \( d \) and \( q \) axis equations [46] as follows:

\[
\begin{aligned}
R_T i_{g,d} + L_T \frac{di_{g,d}}{dt} &= v_{\text{PCC},d} + \omega L_T i_{q} - v_{an,d} \\
R_T i_{g,q} + L_T \frac{di_{g,q}}{dt} &= v_{\text{PCC},q} - \omega L_T i_{d} - v_{an,q}
\end{aligned}
\]  \hspace{1cm} (4.6)

Therefore, the transfer function of the system can be written as follows:

\[
\frac{I_{g,dq}(s)}{V_{an,dq}(s)} = \frac{1}{1 + \tau s}, \quad \tau = \frac{L_T}{R_T}
\]  \hspace{1cm} (4.7)

The converter current controller has transfer function, \( G_c(s) \), which is a PI controller in the \( dq \) reference frame along with the delay, \( \lambda \), contributed by the computation and the PWM represented by transfer function (4.2). This delay is significant as it is normally of the order of 1.5 times the sampling time (\( T_s \)). The controller transfer function is:
CHAPTER IV - CONTROL OF THREE-PHASE POWER FACTOR CORRECTION RECTIFIER

Fig. 4.4: Simplified equivalent circuit of filter and grid impedance.

![Simplified equivalent circuit of filter and grid impedance.](image)

Fig. 4.5: The converter and grid current with PI controller in \(dq\) reference frame.

![The converter and grid current with PI controller in \(dq\) reference frame.](image)

\[ G_c(s) = K_p \left( 1 + \frac{1}{s \tau_s} \right) \]  

(4.8)

where \(K_p\) and \(\tau_s\) are the controller parameters. According to (4.7) and (4.8), \(\tau_s = T_s\) and \(K_p\) is calculated as follows:

\[ K_p = \frac{L_r}{1.5 \alpha T_s}, \quad \alpha \geq 2 \]  

(4.9)

To study the stability of the converter, the impedance based analysis is performed together with the impact of the PCC feedforward compensation [73] and the influence of filter capacitor is also included in the analysis. The analysis of the stability has been thoroughly investigated in Appendix B6. The impact of the PCC feedforward compensation has been also examined in this paper.

The experimental results shown in Fig. 4.5 are the grid current and converter current for different load conditions. Fig. 4.5(a) is the converter and grid current for 25% load and Fig. 4.5(b) shows the current for 100% load. As it can be seen, at low load, the converter current ripple throughout the profile of main current is dominant. More specifically, the impact of switching dead-time is clearer in the low load condition rather than the full load as it is specified with three rectangular dashed lines for both cases.

4.2.1. PR control in the \(\alpha\beta\) reference frame

The schematic of the control system is shown in Fig. 4.6(a). To cancel the steady state error, the stationary or the \(\alpha\beta\) reference frame is used. The control has a voltage outer loop which
provides the references for the inner current controller in the \( \alpha\beta \) reference frame. The converter current controller transfer function, \( G_c(s) \), is now a proportional-resonant (PR) controller along with the delay, \( G_d(s) \), from the computation and PWM defined by (4.2) [69]. The controller transfer function of the fundamental harmonic is as follows:

![Diagram](image)

\( G_c(s) = K_p + \frac{K_i}{s} \)

\( G_d(s) = e^{s\tau} \)

\( K_p \) and \( K_i \) are the proportional and integral gains, respectively.

Fig. 4.6: (a) Implementation of the controller, (b) the current control loop, and (c) the implementation of harmonic compensator in z-domain.
\[ G_c(s) = K_p + K_i \frac{s}{s^2 + \omega_i^2} \] (4.10)

4.2.1.1. Implementation

To compensate for the nonlinearities of the converter due to the blanking time effect, low frequency unwanted harmonics such as 5\(^{\text{th}}\), 7\(^{\text{th}}\), 11\(^{\text{th}}\), and 13\(^{\text{th}}\) which are the largest in magnitude are compensated with resonator controller. The general transfer function is written as follows:

\[ G_c(s) = K_p + \sum_{n=1}^{n} K_{i,h} \frac{s}{s^2 + \omega_h^2} \] (4.11)

The current control loop with harmonic compensators up to 13\(^{\text{th}}\) harmonic is shown in Fig. 4.6(b). In this figure, the feedforward PCC voltage is also added to the current control loop with the gain of \( g_{cc} \) which can be adjusted between 0 and 1. If \( g_{cc} \) is set to zero, the feedforward compensation is removed. The frequency response of the open loop current controller with and without feedforward is shown in Fig. 4.7. The control design is explained in details in Appendix B7.

The implementation of the controller has been done in the \( z \)-domain in view of the digital implementation. To minimize the phase shift introduced by the discretization, the integrator in forward path is transformed to the \( z \)-domain using the forward Euler transform and the integrator in the backward path is transformed to the \( z \)-domain using the Backward Euler transform [71]. Fig. 4.6(c) shows the implementation of the controller in the \( z \)-domain.

To synchronize the system for the unbalance grid, the dual second order generalized integrator (DSOGI) is used. This method is based on the second-order generalized integrator (SOGI). The transfer function of SOGI is expressed as follows:

\[ C(s) = \frac{\omega_r s}{s^2 + \omega_r^2} \] (4.12)

where \( \omega_r \) is the resonance angular frequency. The implementation of DSOGI has been explained in [12] and [13].

Fig. 4.8 shows the controller response with different proportional gains. Fig. 4.8(a) shows a more oscillatory system when the proportional gain is set to 15. Once the gain is reduced to 6.3 oscillatory behavior in the converter becomes more damped as can be seen in Fig. 4.8(b). The comparison between the output of the PR controller for 50\% of the load in Fig. 4.8(b) and the full load response of the PI controller in Fig. 4.5(b), shows better current quality with the PR controller.
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Fig. 4.7: The frequency response of the open loop system for PR controller (a) without and (b) with feed forward ($g_{cc} = 0.8$).

Fig. 4.8: (a) Oscillatory response, (b) more damped response of the grid current for different proportional gains.
4.2.1.1. Compensation

To compensate for the delay caused by PWM, AD conversion and computational delay, compensation has been introduced to the controller for each harmonic compensator. As mentioned, the feedforward compensation effect has been added with the gain of $g_{cc}$ in the system. Therefore, the phase delay in the voltage measurement contributes to the output of the current control. The phase delay impact on the PCC voltage can be written as follows:

$$v_{ff} = g_{cc} |V_{PCC}| e^{j(\theta_{v} + \theta_{v,\text{delay}})} = g_{cc} |V_{PCC}| e^{-j(\theta_{v} + \theta_{v,\text{delay}})}$$  \hspace{1cm} (4.13)

where $v_{ff}$ is the feedforward voltage as it is shown in Fig. 4.6(b). $\theta_{v,\text{delay}}$ is the phase delay which is introduced by the voltage measurement and $\theta_{v}$ could be set to zero.

The output of the HC depends on the measured current as well as the reference current. Therefore, two delays contribute in the path of the HCs; the delay from the measurement plus the delay due to PWM. Then, the output of the HCs as called $v_{\text{Res}}$ (shown in Fig. 4.6(b)) is calculated as follows:

$$v_{\text{Res}} = |V_{\text{Res}}| e^{j(\theta_{I} + \theta_{I,\text{delay}})} = (1 - g_{cc}) |V_{R}| e^{-j(\theta_{I} + \theta_{I,\text{delay}})}$$  \hspace{1cm} (4.14)

In this equation, $\theta_{I,\text{delay}}$ is the phase delay in the current path due to the measurement and the PWM. Since the PCC voltage has contributed to the reference output voltage by the factor of $g_{cc}$, the contribution of the HCs will be $(1-g_{cc})$. The target is to have unity power factor for the converter and therefore $\theta_{I}$ can also be set to zero in (4.14). According to Fig. 4.6(b), the reference output voltage is expressed as follows:

$$v^{*} = v_{ff} + v_{\text{Res}}$$  \hspace{1cm} (4.15)

Ideally, the normalized feedforward voltage (normalized with respect to $V_{PCC}$) has the magnitude of 1 and phase of zero. The difference between the feedforward voltage and the ideal would be the compensation that $v_{\text{Res}}$ must provide.

$$v_{\text{Res,Comp}} = 1 |0^{*} - v_{ff}$$  \hspace{1cm} (4.16)

Corresponding to (4.16), the compensated resonator has an angle denoted as $\theta_{V_{\text{Res,Comp}}}$. Using this angle and the real angle of the resonator without compensation, gives an angle that needs to be added to the current controller for compensation as follows:

$$\theta_{\text{comp}} = \theta_{V_{\text{Res,Comp}}} + \theta_{\text{Res}}$$  \hspace{1cm} (4.17)

According to (4.16), the compensation can be easily added to the block diagram shown in Fig. 4.6(c). Fig. 4.9(a) shows the implementation of the compensation to the HC. For the implementation, the compensation gains are defined as follows:
where $K_{\text{sin},h}$ is the compensation gain for $h^{\text{th}}$ harmonic on the path of the $\beta$-axis and $K_{\text{cos},h}$ is the compensation on the path of the $\alpha$-axis for the $h^{\text{th}}$ harmonic.

Fig. 4.9: (a) the implemented compensation for harmonic compensator, (b) frequency response of the open loop system without phase compensation and (c) frequency response comparison for $13^{\text{th}}$ harmonic.
If in (4.18) the compensation angle is set to zero then the block diagram of the current compensator will be the same as Fig. 4.6(c). Moreover, in (4.18), as the harmonic number increases the compensation gain for the $\beta$-axis increases while the compensation gain for the $\alpha$-axis decreases. The impact of this compensation is more visible for higher harmonics as can be seen in Fig. 4.9(b). For the designed controller, the angle at the 13th harmonic has reduced from 134 degrees to 127 degrees using the compensation method. The importance of this compensation becomes apparent when the number of HCs increases and their resonance frequencies becomes closer to the cross over frequency of the controller.

4.3. DC voltage control loop

The block diagram of the dc voltage control loop is shown in Fig. 4.10. The bandwidth of the voltage controller must be kept smaller than the current controller. The dc link voltage control loop employs a PI controller with anti-windup implementation (not shown) to allow saturation of the current reference during transients.

\[
G_{dc}(s) = \frac{3V_m}{2I_{load}} \frac{1}{C_{dc}R_{load} s + 1}
\]

\[
G_{c,dc}(s) = K_{p,dc} \left( 1 + \frac{1}{sT_{i,dc}} \right)
\]

According to [68], the controller parameters are as follows:

\[
K_{p,dc} = \frac{2V_{dc} \text{ref}}{3\alpha_{dc} T_{in} V_m}
\]

\[
t_{i,dc} = \alpha_{dc} T_{in}
\]

$T_{in}$ has been set to 5$\lambda$ ($\lambda$ is the time delay).

The step response of the system has been plotted for various grid impedances. It should be noted that the target is to minimize differences between the step responses obtained for low-
TABLE 4-1: The parameters of the dc link controller for 2 case studies.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>$L_c = 580\mu\text{H}$</th>
<th>$L_c = 1\text{mH}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{dc}$</td>
<td>5.5</td>
<td>4.2</td>
</tr>
<tr>
<td>$K_{P,dc}$</td>
<td>0.11</td>
<td>0.14</td>
</tr>
<tr>
<td>$t_{i,dc}$</td>
<td>9 msec</td>
<td>4.9 msec</td>
</tr>
<tr>
<td>Overshoot range (%)</td>
<td></td>
<td>1-10</td>
</tr>
<tr>
<td>Settling time range (msec)</td>
<td></td>
<td>9.5-10.5</td>
</tr>
</tbody>
</table>

and high converter-side inductance values. TABLE 4-1 lists the parameters of the dc link voltage controller in order to achieve this similar transient behavior. With reference to Fig. 4.11(a), increasing the grid impedance increases both the overshoot and the settling time.

Fig. 4.11: The performance of dc link control loop (a) general step response for different grid impedances, the transient response of the dc link for (b) 564 V, and (c) 650 V.
However, it is desirable to keep the overshoot no higher than 10% for the largest grid impedance. To study the stability of the converter with the dc link voltage control loop, two different experimental tests have been conducted. Fig. 4.11(b) and (c) show the transient response of the dc link voltage when the controller turns on for linear modulation and overmodulation, respectively.

### 4.4. Experimental results

#### 4.4.1. PFC rectifier connected to Drive

This section is dedicated to the experimental results that have been carried out in the Danfoss Drive A/S laboratory. The experiments have been done by connecting the PFC to a fully SiC based 7.5 kW drive from Danfoss (Danfoss FC302 7.5kW modified drive). For the drive, the switches are all SiC implemented and the maximum switching frequency is 32 kHz. The switching frequency of the PFC is 45 kHz. The PFC is connected via an auto-transformer to the grid. The voltages at grid side are not balanced.

The linearity of the modulation index is extended by adding a zero sequence offset. The calculated zero sequence offset is stored in dSPACE system. The results of this test have been published and explained in Appendix B7.

It can be seen in Fig. 4.12 that to the complete zero sequence offset which is equal to the maximum modulation index $2/\sqrt{3}$ there is a small difference and that is due to that the grid voltage is not balance. To compensate for the unbalance grid, the dc link voltage is slightly higher than normal condition as shown in Fig. 4.13(a). The Drive is connected to a motor test bench which is able to drive the motor generative or regenerative. It should be noted that the results are saved in dSPACE system and plotted in MATLAB.

Two tests have been carried out:

1) The torque is set to zero, and then it increases to 3 N.m and after about 4 seconds the direction of torque changes to -3 N.m. This test shows the bidirectional power flow. The results are shown in Fig. 4.13. As it can be seen, the dc link voltage in all the transitions changes very smoothly. The overshoot in dc link voltage is not noticeable and it reaches to steady state very fast. From Fig. 4.13(b), the direction of the $d$-axis
reference current is changing when the torque changes from positive to negative. In the current also there is not a big overshoot as it is expected. Besides, this test also shows the bidirectional power flow. It should be also noted that applying torque equal to ±3 N.m is equivalent to 50% of PFC nominal power.

2) The torque is set to -6 N.m (regenerative), after 5 seconds the torque becomes zero and after 10 seconds it changes to 6 N.m (generative). Fig. 4.14 shows the results. Again it can be seen that the dc link does not have overshoot and in all the transitions reaches to steady state very fast. In the last transition when the torque changes to 6 N.m, the current overshoot becomes larger than the current limit. Other words, the limit for the current reference has been set to 10 A and it can be seen that $i_d$ is saturated when it reaches to this value. It can also be seen when the torque changes from zero to 6 N.m, for fraction of a second, the measured dc link voltage does not follow the reference voltage. That is because suddenly the demand increases on the load side and until the grid current reaches to the demand the dc link voltage drops from its reference value.

![Fig. 4.13: The experimental results of connecting PFC to Drive, torque from 3 N.m to -3 N.m (I: no torque, II: positive torque, III: negative torque).](image)

![Fig. 4.14: The experimental results of connecting PFC to Drive, changing torque 6 N.m to -6 N.m (I: negative torque, II: zero torque, III: positive torque).](image)
4.4.2. Comparison of the controllers

4.4.2.1. Harmonic evaluation

Due to the nonlinearities of the converter, at low load and high voltage (nominal dc link voltage), the current ripple dominates the main sinusoidal current component based on (3.8). Therefore, the interval over which the current ripple causes rapidly repeated zero crossings increases. In this case, the effect of the blanking time will be more obvious and the current quality after the filtering is unsatisfactory. Fig. 4.15 shows an example of this condition both in simulation and experiments. The test condition is that the dc link voltage is set to 565 V, the grid current is 2 A peak. As it can be seen, the time interval over which the current ripple causes rapidly repeated zero crossings is noticeable. There are two methods to improve the quality of the current at low loads: either increase the converter-side inductance to yield lower current ripple or improve the controller to mitigate the low frequency current harmonics (5th, 7th, 11th, ...). Both methods have been investigated in this work and the results are shown in Fig. 4.16.

In the first scenario, the converter side is increased to 1 mH to yield a 15% current ripple and both the PI and the PR controller have been tested for this case. In the second scenario, the inductance has been kept to yield a 30% current ripple (i.e. 580 μH) and again the two controllers are compared. The experimental results are shown for 25% load and 100% load and the grid current waveform are shown in Fig. 4.16. With reference to Fig. 4.16(b), the grid current with 580 μH inductance and PI controller presents the worst current waveform. A comparison on THD performance is also presented in Fig. 4.17 for both scenarios. The THD of the phase ‘a’ current has been compared.

According to Fig. 4.17, the best harmonic performance is obtained with the PR controller when overmodulation occurs. The reason is that in overmodulation the dc link voltage is better utilized and therefore according to (3.11) the current ripple will be reduced. Unlike overmodulation, the linear modulation applies a larger voltage difference across the converter-side inductance and causes a larger current ripple, thereby causing a more visible effect in the harmonic performance.
Fig. 4.16: The experimental results of the grid current for different controllers and converter-side inductors (a)-(d) 25% of nominal load and (e)-(h) for full load.

With a higher inductance value, the grid regulations for the low frequency harmonics are all fulfilled. However, for a low inductance value, the grid regulations cannot be fulfilled within the low load range using PI controller. In line with the objective of the project, the lowest possible inductance value will eventually be chosen that yields an acceptable harmonic performance at low frequencies. Using PI controller in this case shows weak harmonic performance in comparison with PR controller for 580 $\mu$H. And that is the break point for the efficiency and the impact of controller on the efficiency at low loads.
Fig. 4.17: The harmonic evaluation of the controllers with two different inductance value (a) $L_c = 1 \text{ mH}$, (b) $L_c = 580 \mu\text{H}$.

4.4.2.2. Efficiency evaluation

The efficiency of the converter has been measured for both of the controllers to evaluate the effect of these controllers on the conversion efficiency. The measurement was carried out using a YOKOGAWA-WT3000 precision power analyzer for both the ac and dc sides. The linear average mode of the measurement is active and taking averaging over 128 cycles. The accuracy of the measurement for a 2 A current or lower (less than 20% load) is about 0.05% and for higher than 2 A is about 0.00055%. Similarly, the voltage accuracy for the ac-side voltage (peak of 325 V) is 0.00325% and for dc-side is 0.007%. After operating the system for 45 minutes, the full load efficiency was measured. After 3-5 minutes, the measurement for each load step was performed to make sure that the converter reached the steady state. Fig. 4.18 shows the experimental setup for the efficiency measurements. It should be noted that for monitoring the accuracy of the measurements at the dc side, two precision multi-meter (Agilent 34410A) have been used. For the dc current measurements, a high precision current sensing resistor (precision 1 ppm/°C) was used for monitoring purpose. These two multi-meters are synchronized with the power analyzer. The results using only the power analyzer or using both the power analyzer for the ac measurement and the multi-meter for the dc measurements are identical.
Fig. 4.18: The experimental setup for measuring the efficiency.

Fig. 4.19: The measured efficiency with and without diode at low load (25% < Load < 40%) for the PR control (without including drive loss).

Fig. 4.20 shows the measured efficiency of the converter obtained with the PI and the PR controllers (black and gray lines, respectively). The efficiency measurement has been conducted in 4 different scenarios. Firstly, both controllers have been compared regarding their impact on efficiency and secondly the SiC Schottky diodes have been removed and the efficiency measurement repeated for both controllers. Due to the presence of the SiC Schottky diodes, the total output charge of the diodes is added to the output charge of MOSFETs and certainly the capacitive switching loss increases. Adding the SiC Schottky diodes adds about 68 nC to the capacitive charge of the MOSFETs and it increases the capacitive loss from 2.6 W for one switch to 4.56 W. This increase causes a reduction of about 0.2% as idle loss. This reduction can easily be seen in Fig. 4.19 at low load. The impact of diode for the whole range of loads for two different controllers is also shown in Fig. 4.20.

The presence of the Schottky diode at higher loads is not so evident. The forward drop voltage of the body diode is smaller than the Schottky diode and the current at higher loads will flow mostly through the body diode rather than the Schottky diode.
The maximum efficiency occurs at 55% of the load for both of controller. For the PR controller the maximum achievable efficiency is 99.1% and for the PI controller it is 99.08%. As expected, because of better harmonic performance of the PR controller at lower load a higher efficiency is achieved. Also, when the load is increased, the efficiencies obtained with the two controllers become closer.
CHAPTER IV- CONTROL OF THREE-PHASE POWER FACTOR CORRECTION RECTIFIER

The other observation for the efficiency curve is that with and without the anti-parallel diode the efficiency is substantially flat for a wide range of loads. The efficiency at full load for both cases is around 99%.

4.5. Summary

The following is a list of the main conclusion and summary that can be drawn from the analyses presented in this chapter:

- Adding the PCC voltage to the control input is equally beneficial when using the PI or PR current controllers;

- At low loads and high dc link voltages, the power quality is the lowest. Because, the current ripple in the converter-side inductor is relatively large compared to the main fundamental current and the effect of switching dead-time becomes more visible.

- The PR controller with harmonic compensation allows the value, and hence the size of the converter-side inductor, to be reduced by a factor of 2/3.

- The measured conversion efficiency of the 5 kW SiC based three-phase PFC at half of nominal load is about 99.1% and at full load it is 98.95%.

- Using SiC Schottky diodes anti-parallel with the MOSFETs increases the switching loss by a factor of 70% for each switch. The contribution of the diode at high load is very small because the forward voltage drop is higher than the SiC MOSFET body diode.

- The impact of using different controllers on the efficiency is more obvious at low loads. The PR controller shows better harmonic performance at low load than the PI controller. Therefore, the efficiency at low load is also higher for the PR controller.

- Bidirectional power flow is provided for this converter and the performance is tested by connecting the PFC converter to drive.

- The efficiency achieved is greater than the efficiencies most recently reported in the literature representing the state of the art (see Chapter 2).
5. Conclusion and Future work

5.1. Conclusion

This PhD research work has presented a comprehensive design of a two-level three-phase power factor correction (PFC) using silicon-carbide (SiC) devices to further increase efficiency. To achieve the compliance with the grid standards (e.g. IEEE-519) an $LCL$ filter has been used for the PFC. A complete model of the filter is achieved by analyzing the current and voltage waveform of each filter parameter. The converter current ripple has been analyzed to choose the converter-side inductance. The analysis results are as follows:

- The converter current ripple waveform is generalized by categorizing its behavior into two intervals with respect to the grid period. Interval 1 is $0 < \omega t < \pi/3$ and interval 2 is $\pi/3 < \omega t < \pi/2$.

- Each time interval has its own maximum current ripple. For the first interval, the maximum current ripple occurs at zero crossing. For the second interval, peak current contains the maximum current ripple. For modulation index higher than 0.845, the maximum current ripple occurs at zero crossing; otherwise, it occurs at peak current.

- A general equation has been derived for the maximum converter current ripple. This expression is generalized for both the sinusoidal PWM and the third harmonic injected PWM (THPWM).

Since the converter-side inductor is exposed to high frequency current ripple, the inductor design is critical. MPP Powder core material is used, due to the low power loss and also lower dependency on the dc pre-magnetization. For a 5 kW three-phase PFC, solid wire for winding of this inductor is the best compromise between the simplicity and the loss. The ac copper loss for switching side-band harmonics and its multiples is negligible in comparison with the ac copper loss at the fundamental frequency.

Using the analysis for the converter current ripple, a minimum and a maximum margin for the filter capacitance have achieved. The upper margin is defined by the absorbed reactive power and the lower margin is achieved as a function of the maximum converter current ripple. It is shown that even at low switching frequency (e.g. 10 kHz) the lower margin of the filter capacitance is about half of the upper margin.

Line impedance stabilization network (LISN) provides a fixed impedance for the current harmonics (at switching side-band harmonics and multiples). To optimize the grid-side filter inductor, LISN is connected between the grid and the converter. The filter inductance is derived as a function of the LISN impedance. The only way to find the minimum size of the grid-side filter is using LISN, despite changing of the grid impedance. Using LISN also assures that the measurements are repeatable.
To achieve the maximum efficiency, the loss distribution in the converter is analyzed for different switching frequencies. Therefore, the switching frequency is selected to be in the range of 45-50 kHz. Respecting electromagnetic interference (EMI), 45 kHz has finally been selected as the switching frequency. According to the selected switching frequency, an LCL filter is designed and the layout is optimized for a 5 kW three-phase PFC using SiC MOSFETs.

Two types of current controllers are used: 1) PI controller in the rotational reference frame and 2) Proportional-resonant (PR) controller in the stationary reference frame. The effect of adding the point of common coupling (PCC) voltage to the current controller is studied (i.e. feedforward compensation). The observations of studying the controllers are as follows:

- PI controller without harmonic compensation (HC) needs larger filter to obtain the same harmonic performance as PR controller.

- With the same filter, the efficiency of the converter with PR controller is higher at low loads.

The efficiency of the converter is measured for different scenarios. The efficiency is measured with the PI controller and the PR controller. The efficiency is also measured with and without SiC Schottky diode in parallel with the SiC MOSFETs. The following results are achieved:

- The efficiency of the converter is higher without using the SiC Schottky diodes.

- For PR controller, a maximum efficiency of 99.1% is achieved at 50% of nominal load. The measured efficiency at full load is 98.95%.

- The conversion efficiency is substantially flat for a wide range of loads for both controllers.

The major contributions of this work can be summarized as follows:

- A complete analytical model for an LCL filter of two-level PFCs has been proposed. This model can be extended for the multilevel converters. By using this model:
  - Comparison between two-level and multilevel converters is analytically possible.
  - Comparison between the size of the filter for different modulation schemes is possible.

- A high efficiency two-level PFC using SiC switches with the maximum efficiency of 99.1% has been achieved.
5.2. Future work

The following future work is suggested:

- Investigating active damping for the presented converters;

- Studying the impact of different modulation schemes on the efficiency and size of the filter;

- Measure the efficiency of the converter in the bidirectional operation;

- Analytical common mode filter design for PFCs;

- In this PhD work, a three-level PFC using Gallium-Nitride (GaN) switches has also been designed. The design process and specifications of the designed converter have been described in Appendix A. Comparing the two-level SiC based converter from different aspects with three-level GaN based converter can be very interesting. Filter size, EMI performance, and efficiency are the main interests of this comparison.
References


[37] Hitachi Metals, Powerlite C-Cores, 2605SA1.


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[81] How to fine tune your SiC MOSFET gate driver to minimize losses, App. Note AN4671, pp. 1-17.


A. Three-Level Three-Phase Power Factor Correction Rectifier

This chapter presents a hybrid three-level converter which utilizes generalized multilevel concept to achieve low power losses and equally distributed losses among the active switches. In generalized three-level converter and active neutral point clamped converter (ANPC), six active switches are employed. Using this switching strategy, only two of six switches are switched with high frequency and the rest are switched with low frequency (i.e. grid frequency). Therefore, two different frequencies bring an opportunity to use two different technologies for switches. For two high frequency switches, low switching loss-high frequency gallium-nitride (GaN) FET is used which helps more to reduce the switching loss. For low frequency switches, the conventional silicon MOSFET is employed.

A. 1. Introduction

Multilevel converters have become interesting solution for high voltage, high power applications [93]-[102]. Lower common mode voltage, lower stress on power semiconductors, and higher quality of current and voltage have changed them into serious rivals of two-level converters [93], [94]. Although neutral point clamped converter (NPC) was firstly proposed for medium voltage industry applications, this topology is now used for low voltage drive applications as well. However, this topology among all its advantages offers one substantially weakness which is an unequal distribution of the switching loss between the power semiconductor devices. To overcome this problem, active NPC (ANPC) is introduced to share the losses between active switches equally, even though number of active switches is increased from 4 to 6 in three-level ANPC [95], [96]. In 2001, Peng presented a general topology of multilevel converter in which NPC, flying capacitor and ANPC converter can be driven from that topology and is called generalized multilevel converter [95]. This topology has interesting features that can be used to improve the overall efficiency of multilevel converters. In [98], a new topology of 5 level converter has been proposed which uses the idea of NPC and flying capacitor to generate five level converter. In 5 level ANPC (5L-ANPC), there are two different switching frequencies, the higher voltage switches are switching with grid frequency and the lower voltage switches are switching with higher frequency. Therefore, the switching loss in high voltage switches is almost negligible and only their conduction loss contributes to the overall loss of the converter.

GaN FETs are not commercially available for high voltage which makes them suitable for multilevel applications. Combining the idea behind generalized multilevel concept or 5L-ANPC, and different semiconductor technology can be beneficial from conversion efficiency as well as power density of the converter. This work uses this combination and is built a hybrid ANPC (HANPC) in which GaN FETs are used for high frequency switches and normal Si are used for low frequency ones.
A. 2. Three-level ANPC

The schematic of a three-level active NPC is shown in Fig. A.1. Switches S1-S4 are the low frequency switches and Q1 and Q2 are the high frequency switches. When the voltage reference is positive, switches S1 and S3 are in turn-on state. When Q1 is turn-on, the ac link is connected to the positive rail and when it is turn-off, the path of the current is correspondingly provided via S3 and Q2 and the connection to the dc link midpoint is achieved. Similar scenario can be explained for negative reference voltage, when the complementary of S1 and S3 are now in turn-on state (i.e. S2 and S4). In this case, when Q1 is turn-on, the zero state is provided and when Q2 is turn-on the negative rail is connected to the ac link. Although there are 6 active switches in each leg, sever switching losses occur only for two high frequency switches and the other 4 switches are not facing high switching frequency loss. The switching states have been listed in TABLE A-1 [98].

A. 3. Hybrid three-level ANPC

In ANPC, existing two switching frequencies leads to use two different types of switches. Therefore, for Q1 and Q2, GaN FET is interesting choice. For low frequency switches, Si MOSFET can be employed in the circuit. Therefore, this converter is called hybrid active NPC (HANPC). To demonstrate the performance and superiority of HANPC, a 10 kW three-

<table>
<thead>
<tr>
<th>State</th>
<th>S1 &amp; S3</th>
<th>S2 &amp; S4</th>
<th>Q1</th>
<th>Q2</th>
</tr>
</thead>
<tbody>
<tr>
<td>State “+”</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0 (positive half cycle)</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0 (negative half cycle)</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>State “—”</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
TABLE A-2: The converter specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{nom}$</td>
<td>Nominal power</td>
<td>10 kW</td>
</tr>
<tr>
<td>$V_{ac}$</td>
<td>Ac voltage</td>
<td>230 V</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>DC link voltage</td>
<td>650 V</td>
</tr>
<tr>
<td>$f_{g}$</td>
<td>Grid frequency</td>
<td>50 Hz</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>Switching frequency</td>
<td>100 kHz</td>
</tr>
<tr>
<td>$L_c$</td>
<td>Inductance</td>
<td>133 $\mu$H</td>
</tr>
<tr>
<td>$C_{dc}$</td>
<td>DC link capacitor</td>
<td>144 $\mu$F</td>
</tr>
</tbody>
</table>

A phase hybrid generalized three-level converter has been built. The specifications of the converter are listed in TABLE A-2. This converter consists of two GaN FETs- 650 V, 60 A- and four Si MOSFETs- 650 V, 130 A. The schematic of one leg of the converter (i.e. 3.3 kW single phase schematic) along with the built prototype are shown in Fig. A.2(b). The advantage of using high voltage GaN is that there is no need for antiparallel diode. Because, firstly GaN FETs are capable of reverse conduction even though they do not have parasitic body diode construction. Secondly, by adding another diode in parallel with switch, the output capacitive charge of the switch increases and it increases the switching loss. In addition, the reverse conduction of GaN FETs does not have recovery losses which means during the dead time between Q1 and Q2 the transition is lossless.

A. 4. Loss distribution

A. 4.1. Inductor design and loss calculation

The converter works in the linear region of the modulation index. The process of calculating the current ripple is very similar to the one which is presented for two-level PFC in Section 3.3.1.

Fig. A.2: (a) the schematic of one phase of three-level HANPC, (b) the build prototype of one leg three-level HANPC.
Using these time intervals, the current ripple can be obtained as \[\Delta i = \frac{V_{dc}}{12f_{sw}}(2 - m_a)(3m_a - 2)\] (A.1)

By determining the desired maximum current ripple, the minimum inductance value can be achieved. According to, the maximum current ripple depends on the modulation index square and also the dc link voltage level. In PWM converters, the intention is to work at high modulation index to utilize the most of the dc link voltage.

To have 20% of the nominal current as current ripple in the converter with the specification that is mentioned, the required inductance value must be 133 \(\mu\)H. For designing the inductor, iron power Kool-Mu EE core- K5528E060- is chosen with solid winding. The number of winding is 33 turns which gives 136 \(\mu\)H at full load and 235 \(\mu\)H at no-load. The designed inductor is shown in (c). The ac resistance has been measured at switching frequency and its multiple (where the current harmonics happen) and are listed in TABLE A-3. The measurement has been done using precision impedance analyzer Agilent 4294A. For the accuracy in measurement, the ac resistance of the winding is measured with the air core. From TABLE A-3 although the ac resistance at high frequency is way bigger than the fundamental frequency, the loss is almost negligible compared to fundamental.

The expected core loss in this core at full load condition is calculated to be 1.35 W for each phase inductor. The core loss has been calculated for each switching cycle and for each \(B-H\) curve in one switching cycle as suggested in Chapter 3.

A. 4.3. Loss in the switches

For calculating the switching capacitive loss and conduction loss of the switches, the presented method in Section 3.6 is used. Since the MOSFETs are switching with grid frequency the switching capacitive loss is negligible and therefore is not reported in this Section. The switching parameters are listed in TABLE A-4. According to the parameters and the full load condition, the switching capacitive and conduction losses are calculated for each leg as listed in TABLE A-5. Even though the total gate charge of Si MOSFET is about 30 times larger than the one of GaN FET, the drive loss for both of them is negligible.

A. 4.2. Total loss

To calculate the total loss in the converter, the presented method in Section 3.6 is used. The total loss is summation of switch losses and inductor loss. The total loss at full load condition
TABLE A-4: The switching parameters of Si MOSFET and GaN FET.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>GaN</th>
<th>Si</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{on @ 50^\circ C}$ (mΩ)</td>
<td>40</td>
<td>17.5</td>
</tr>
<tr>
<td>$Q_{oss}$ (nC)</td>
<td>106</td>
<td>4100</td>
</tr>
<tr>
<td>$Q_g$ (nC)</td>
<td>12</td>
<td>363</td>
</tr>
</tbody>
</table>

TABLE A-5: Loss in the switches.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Loss (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{swQ1} = P_{swQ2}$</td>
<td>1.85</td>
</tr>
<tr>
<td>$P_{cond. Q1&amp;Q2}$</td>
<td>9</td>
</tr>
<tr>
<td>$P_{drive. Q1&amp;Q2}$</td>
<td>0.0084</td>
</tr>
<tr>
<td>$P_{cond.S1-S4}$</td>
<td>4</td>
</tr>
<tr>
<td>$P_{drive. S1-S4}$</td>
<td>0.0003</td>
</tr>
<tr>
<td>$P_{total}$</td>
<td>16.7</td>
</tr>
</tbody>
</table>

is 0.7% and the distribution of losses in the system is shown in Fig. A.3. As it can be seen, the major loss in high power is the conduction loss and switching loss.

A. 5. Conclusion

This chapter has investigated a 10 kW GaN based hybrid three-level active NPC (HANPC).

- Using the presented method in Chapter 3, the filter parameters, especially the converter-side inductor can easily be calculated.
• The inductor for this converter is designed and the core loss and copper loss is calculated.

• 6 active switches are utilized in this converter. Due to the superior advantages of GaN switches the switching frequency of GaN FETs are set to 100 kHz.

• Even with this switching frequency, the switching capacitive loss only occupies 16% of the overall loss in the converter.

• Expected efficiency of the converter at full load is 99.3%. GaN FETs are switched with 100 kHz and Si MOSFETs with 50 Hz switching.

• The majority of the power loss is dedicated to the conduction loss in both GaN and Si switches.
B. Appendix B

Appendix B includes the selected published papers as a part of the PhD work listed as follows:


