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Procedure to compare different design methods for implementation-ready high power inductors

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***Abstract*—In order to realize efficienct high power inductors with high power density, different design methods should be compared. This paper proposes a design procedure where different design methods are compared to find appropriate inductor designs for any given specification. Three design methods are compared in a 10kW and 20kW scenario. The three design methods differ in the choice of core material and winding type. The two chosen core types are ferrite cores and powder cores, and the two chosen winding types are copper foil and PCB. In the two scenarios, the design method that obtains the largest power density for the same efficiency, are when ferrite cores and PCB windings are utilized. In the 10kW scenario, up to 32% increase in power density is achieved for the same effiency when using the best design method compared with the second best. In the 20kW scenario, up to 38% increase in power density is achieved for the same effiency. Two inductor solutions are presented using ferrite core and PCB, and both have half-power efficiencies of approximately 99.9% at the inductor worst case operation point.**

***Index Terms*—Inductor design, pareto analysis, dc-dc converter, planar inductor, planar magnetics, pcb windings, foil windings.**

I. Introduction

Inductors are an essential component in any switched-mode power supply (SMPS) topology. Inductors are typically one of the most bulky components in SMPS [1], [2]. Therefore, to have a SMPS with high power density and high efficiency, optimized inductors are a necessity. This is especially true for large output power applications, where the magnetic components dominate the size of the entire SMPS [3].

There are many type of inductors, some operate only in the ac domain like ac/dc converters [4], while others have an influence of dc bias like in dc/dc converters [5]. An optimal inductor design changes drastically depending on the application. A tool is therefore needed to quickly examine the various design methods and find the most optimal for the given specification. To investigate the potential of an inductor design method for a given specification, pareto analysis is a useful tool [6], [7], [8]. The problem with a true pareto analysis is that it usually utilizes assumptions, weighing factors, non-existing components, etc. to investigate the potential of a given design method. Often physical restrictions that are placed on real inductors are ignored in pareto analysis. These include e.g. not being able to lay the windings in the theoretically chosen winding configuration, or not having a specific magnetic core size and shape. The type of pareto analysis that excludes these physical restrictions are therefore theoretical and not implementation-ready designs.

This paper introduces a design procedure to compare different design methods for power inductors. It is chosen to only compare inductors under the influence of dc bias, meaning inductors suited for dc/dc converters and applications alike. The design procedure is presented in section II. Three design methods are presented in section III, and the loss model used in the design methods are presented in section IV. In section V, the design methods are used to design several inductors and plot them with their half-power efficiency as a function of power density. The design methods are afterwards compared with one-another. The paper is concluded in section VI.

II. Design procedure for inductors with dc bias

The inductor design procedure that is presented in this section, is made for inductors with dc bias and are placed in dc/dc converter buck topologies. The inductor is placed in the output filter of dc/dc converter buck topologies, making the output filter a LC circuit as illustrated on Fig. 1. It should be noted that the design procedure is not limited to only include buck-topology inductors with dc bias, but it is chosen only to present those in this paper.

The proposed inductor design procedure are shown on Fig. 2. The flowchart of Fig. 2a is an illustration of the top level of the program (henceforth called the master program). In the flowchart, the *Specification requirements* are all the data related to the application, in which the inductor are intended to operate, e.g. output voltage, frequency, duty cycle

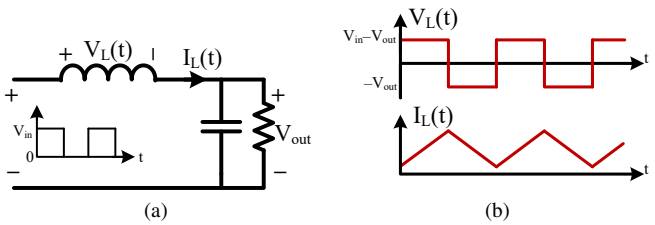


Fig. 1. LC output filter of a buck topology dc/dc converter

etc. The *Choose core* loop indicates that the master program designs different inductors with all available cores, for the same specification. The *Design method* blocks, are different methods for designing the inductor, where multiple solutions will be produced. The different solutions, has different e.g. number of turns, air gap etc. The master program saves the optimal solution for each design method. Multiple design methods can be added to the master program, allowing for quick comparison of any design method. It is important to note that the design procedure of this paper is not meant for obtaining the most optimal inductor design, rather simply to compare the most optimal solutions of the different design methods.

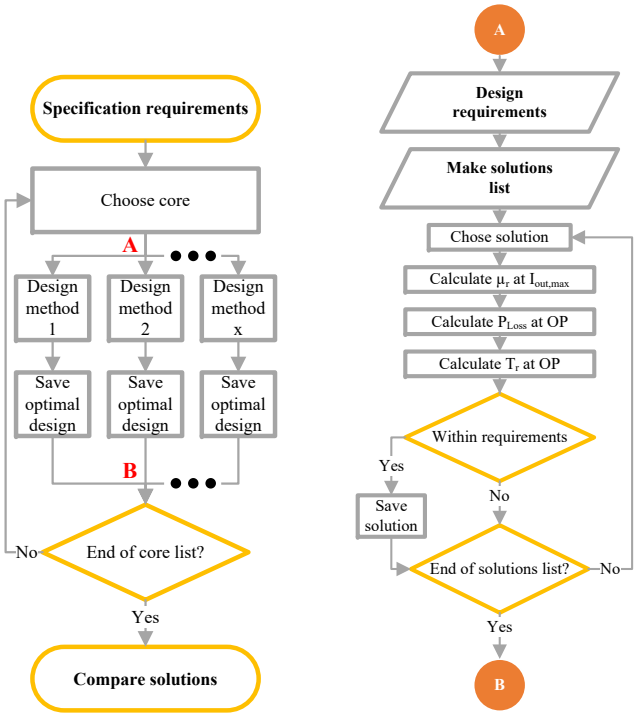
The design procedure of all the design methods are modeled the same, and the design procedure is shown on Fig. 2b. The design methods all have their own specific requirements (henceforth called design requirements), and should be set specifically for every design method. In the flowchart, the *Make solution list*, finds all possible configurations for the winding arrangement within the core. Thereafter, the design method checks if the solution is valid, by verifying that all of the calculation results are complying with the specification requirements and the respective design requirements. Among many validations, one is to calculate the relative permeability (μ_r) at maximum current (I_{out}) in order to be within the requirements and to be outside of saturation. Another validation is the calculation of the power loss (P_{Loss}) and temperature rise (T_r) at the inductor worst-case operation point. If a solution passes all of the validations, then the wanted results of the solution is saved for a single point, which is at an optimization point (OP) chosen by the user.

III. Description of the Design Methods

Three different design methods are presented in this paper for comparison. Multiple can be added, but for illustration of the design procedure, the design methods are limited to three. Any core type can be added, but to limit the amount of data, only E-cores and planar E-cores are considered in the design procedure. The three design methods are:

Design method 1: Powder core with copper foil winding
Design method 2: Ferrite core with copper foil winding
Design method 3: Ferrite core with PCB winding

Design method 1 is where powder cores are considered as the core material. Powder cores contains distributed air gaps, thereby removing the need for manually inserting an air gap. The distributed air gap within the core produces a soft drop in inductance with the dc-current. Design method 2 and 3 use ferrite cores, having a need for an air gap in the core. For simplicity, the air gap has been restricted to always be placed on the middle leg of the core. The air gap introduces fringing losses. To reduce the fringing losses, all of the windings are placed one air gap length away from the middle leg of the core. The fringing losses are therefore assumed to be small in value



(a) Master program (b) Design method

Fig. 2. Flowcharts of the design procedure used in the programs, where OP are the Optimization Point of the inductors

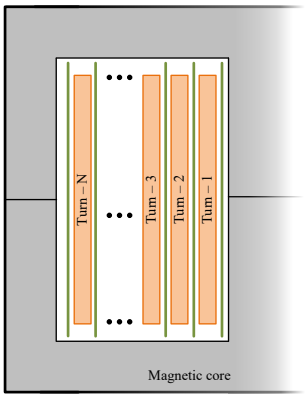
and therefore negligible. Each ferrite core has a restriction on the allowed air gap, based on commercially available E-cores. This restriction has been modeled by an empirical equation, and included in the design methods. The empirical equation is based on the dimensions of the middle leg of a given E-core, and it is calculated as:

$$l_{gap,max} = 1.151\mu m + 0.01815 \cdot L_d + 1.639 m^{-1} \cdot A_d \quad (1)$$

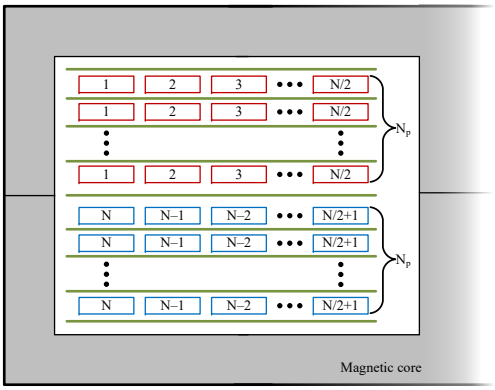
Where $l_{gap,max}$ is the maximum allowed air gap, while L_d and A_d is the length and cross-sectional area of the E-core middle-leg. All the dimensions are in si-units.

The winding configurations of the design methods are limited to those shown on Fig. 3. For copper foil windings, only the winding configuration with stacked winding-turns are considered, as illustrated on Fig. 3a. For PCB windings, the winding configuration of Fig. 3b is utilized, meaning that half of the winding-turns (N) should fit on a single layer. By parallel-connecting many layers (N_p), all of the window area is utilized.

All the inductor designs are aimed to be physically possible to make. To this end, many physical restrictions are placed in the design requirements, including distance between layers, bobbin thickness (h_{bob}) etc. All the distances are illustrated on Fig. 4, and the corresponding values are listed in Table I. h_{bob} is chosen based on the commercially available best fitted bobbin for the core.



(a) Copper foil wound inductor



(b) PCB wound inductor

Fig. 3. Illustrations of how the windings are placed in the window area of the inductor core

IV. Inductor Loss Model and Parameters

This section covers what is performed by the blocks *Calculate P_{Loss} at OP* and *Calculate T_r at OP* from the flowchart on Fig. 2b. First are the inductance at the optimization point (OP) calculated as [9]:

$$L = \begin{cases} A_L \ N^2 \ \mu_{i\%} & \text{Powder cores} \\ \dfrac{\mu_0 \ \mu_r \ A_e \ N^2}{l_e + l_{gap} \ (\mu_r - 1)} \ K_f & \text{Ferrite cores} \end{cases} \tag{2}$$

Where L is the inductance, A_L is the inductance factor and N is the number of winding-turns in the inductor. A_e and l_e are the effective core cross-section and effective core magnetic path length, respectively. μ_0, μ_r and $\mu_{i\%}$ is the permeability of free space, the relative permeability of the core and the dc bias reduction of permeability respectively. K_f is the fringing factor defined as [9]:

$$K_f \ = 1 + \frac{l_{gap}}{\sqrt{A_e}} \ \log\left(\frac{2 \ h_{wa}}{l_{gap}}\right) \tag{3}$$

Where h_{wa} is the height of the core window area.

The power loss in the inductor (P_{Loss}), can be split into two parts; winding loss and core loss. The winding loss are calculated as a sum of the dc and ac winding loss [5]. The core loss is calculated by using the improved Generalized Steinmetz Equation [10]. The fringing loss and capacitive loss of the inductors are assumed negligible and are not included.

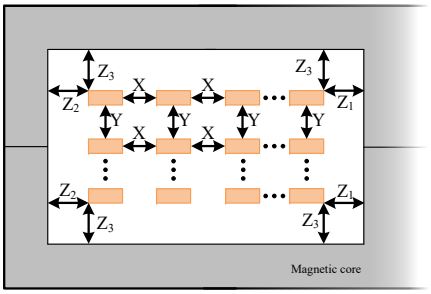


Fig. 4. Illustration of the inductor core window area, where the requirements of Table I are depicted

TABLE I
Design Requirements

	Distance to turns		Distance to core		
	X	Y	Z_1	Z_2	Z_3
Foil	55µm	0	*	1mm	1mm
PCB	0.5mm	0.1mm	**	0.5mm	0.1mm

* if $h_{bob} \geq l_{gap}$ then $Z_1 = h_{bob}$ else $Z_1 = l_{gap}$
** if 0.5mm $\geq l_{gap}$ then Z_1 = 0.5mm else $Z_1 = l_{gap}$

The method of calculating the temperature rise should be determined by the cooling method that is chosen in the design procedure. For all of the design methods, it is assumed that the inductors are naturally cooled, meaning that the heat transfer will be from the inductor to the surrounding air. For this purpose, an empirical equation is used [11]:

$$T_r = \left(\frac{P_{loss} \cdot 10}{A_{su}}\right)^{0.833} \tag{4}$$

Where T_r is the temperature rise of the inductor and A_{su} is the surface area of the inductor. It should be noted that the choice of cooling method greatly influences the solutions of the design methods. For instance, if instead a heat sink is applied to the inductor core, then a planar E-core is much better cooled than a normal E-core.

To obtain temperature dependency on the inductor parameters and power losses (e.g. from the resistivity of copper), all of the calculations of this section are iterated. The iteration stops when two consecutive temperature rise iterations are within 1% of each other.

V. Results of the Design Procedure Program

The design methods from the previous sections are tested in this section, and results of the inductor efficiency and power density are presented for all three design methods. All the cores that are used in the analysis are from Magnetics, and for ferrite core materials, only R, P and F are considered. For the powder cores, only Kool Mµ are used with relative permeabilities; 26µ, 40µ, 60µ and 90µ.

The chosen optimization point for all the designs are at half output power. The term half output power is vast, since many combinations of output voltage and output current equals half output power. The chosen optimization point in this paper is at maximum output current and half output voltage, see Fig. 5 for an illustration. The chosen optimization point is at the worst-case operation for buck topology inductors.

Fig. 6 is an example of a set of data, illustrating how the data solutions of the design methods are represented. All the different inductor designs that satisfy the requirements of the investigated design method, are shown with blue dots. This means that there only is one blue dot on the figure for any chosen core size and type. A change in core material does however produce another solution, even if it is the same core size and type. The red line shows the most optimal designs with respect to efficiency, and it is this line that is compared with the other design methods. The same procedure is done for every design method and every specification requirements that are entered into the master program. The power density of the inductor designs are calculated from the maximum output power of the specification compared with the volume of the core. The volume of the windings are neglected in all power density calculations.

A. *Comparison of the three design methods*

Two scenarios are used for comparing the three design methods. The specification requirements of the scenarios are listed in Table II, where the only difference are the maximum output power and maximum output current. The results from the two scenarios are shown on Fig. 7. It follows that design method 3 is slightly superior at almost every point on the curves, whereas design method 1 is worst for all points. By comparing design method 2 and 3, it follows that for the same efficiency, design method 3 obtains up to 32% and 38% larger power density in scenario 1 and 2 respectively.

B. *Output power sweep with design method 3*

Since design method 3 is always superior in the chosen scenarios, it is chosen to compare design method 3 with itself for different output power levels. On Fig. 8a a comparison is made for different output power levels, where it is the maximum output current that is changed in the specifications.

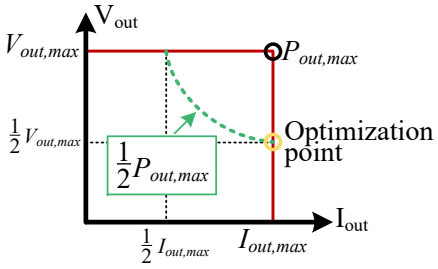


Fig. 5. Illustration of the capability graphs that are used in the design method, along with a marked optimization point

TABLE II
SPECIFICATION REQUIREMENTS

Parameter	Scenario 1	Scenario 2
Maximum output power ($P_{out,max}$)	10kW	20kW
Input voltage (V_{in})	710V	710V
Maximum output voltage ($V_{out,max}$)	700V	700V
Maximum output current ($I_{out,max}$)	14.29A	28.57A
Inductor frequency (f)	200kHz	200kHz
Maximum temperature rise ($T_{rise,max}$)	50°C	50°C
Ambient temperature (T_{amb})	40°C	40°C

It follows that for the same efficiency, the power density rises with the output power level. It also follows that at low output power, all of the possible solutions are located in the low power density region. This can be explained from the specification requirements. Since only the maximum output current is changed when changing the maximum output power, it follows that the inductor designs becomes voltage dominated at lower output power levels. Voltage dominated designs require many winding-turns to reduce the idle losses in the inductor. Since many turns are required, larger cores are needed to fit the amount of turns inside the cores window area. The power density is therefore both reduced by the resulting large core sizes and the lowered output power level.

Alternatively if the output power is changed by adjusting the input voltage of the inductor while maintaining the same output current, then at low output power levels, it is current dominated designs. The results of such a system is shown on Fig. 8b, where it follows that for the same efficiency, larger power densities can be obtained at low output power in a current dominated design, compared with a voltage dominated design. It is however still the case that for the same efficiency, the power density rises when the input voltage is increased.

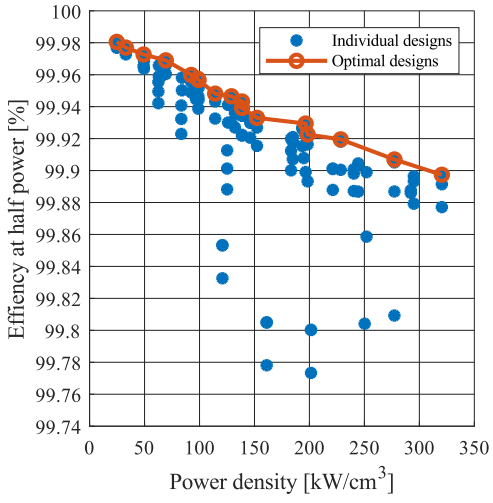
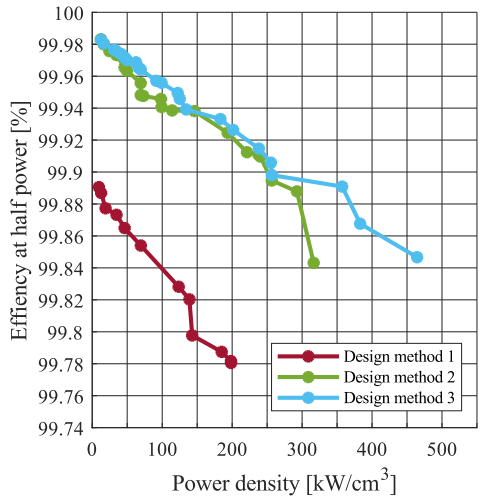
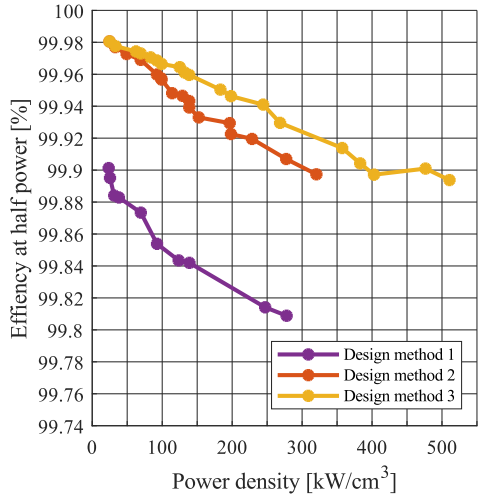


Fig. 6. An example of an output file from the master program. The blue dots are the half-power efficiency of all the valid inductor design solutions, while the red line is the most optimal designs with respect to the efficiency

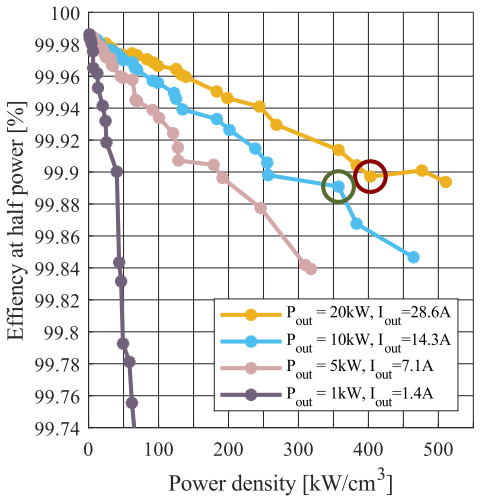


(a) Scenario 1

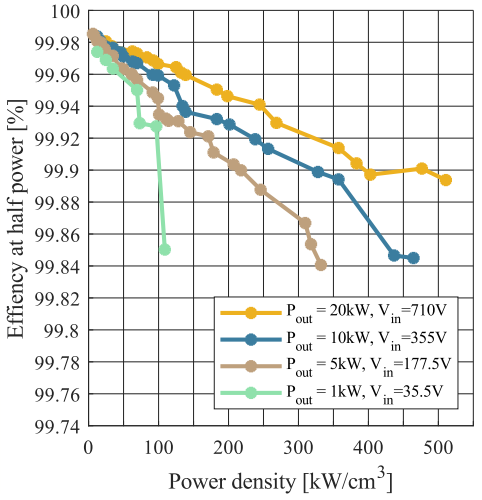


(b) Scenario 2

Fig. 7. Comparison of the three design methods for the scenarios described in Table II



(a) Changing output current, constant input voltage of 710V



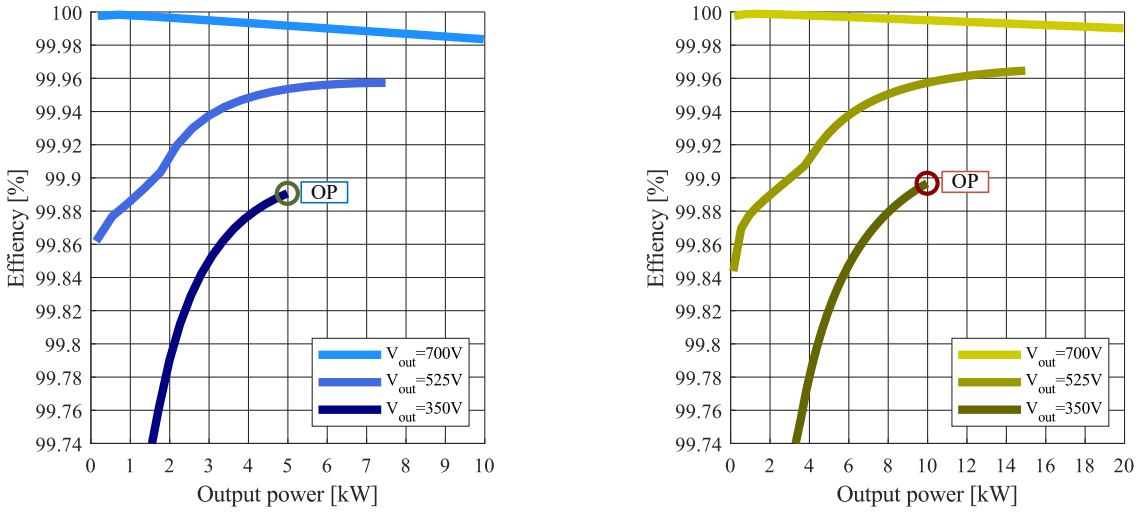
(b) Changing input voltage, constant output current of 28.6A

Fig. 8. Comparison of several scenarios using design method 3, where the output power level is changed by either changing the input voltage or the output current

On Fig. 8a there are two circles on the 10kW and 20kW curves respectively. These circles each indicate an inductor design solution. For convenience the 10kW solution are referred to as solution 1, while the 20kW solution are referred to as solution 2. The design specifications for the two solutions are listed in Table III, and the efficiency curves of solution 1 and 2 are shown on Fig. 9a and 9b respectively. The efficiency curves are obtained by using inductor duty cycles of 0.986, 0.739 and 0.493 for the output voltages of 700V, 525V and 350V, respectively. Both solutions obtain almost 99.9% efficiency at the optimization point which is at the worst-case operation point for buck-type inductors.

TABLE III
SPECIFICATIONS OF THE TWO INDUCTOR DESIGN SOLUTIONS

Parameter	Solution 1		Solution 2	
Magnetic core	FR44310EC		FR45810EC	
Number of stacked cores	2		2	
Volume of core (V_e)	28000	mm^3	49600	mm^3
Number of turns (N)	12	turns	8	turns
Height of turns (h)	210	µm	175	µm
Breadth of turns (b_w)	1.55	mm	4.55	mm
Mean-turn-length (l_w)	19.16	cm	28.11	cm
No. of parallel connections (N_p)	15		20	
Air gap on center core leg (l_{gap})	0.9	mm	1.20	mm
Inductance at max. output current (L_{min})	101.56	µH	46.09	µH
DC resistance (R_{dc})	8.06	mΩ	2.42	mΩ
AC resistance at inductor frequency (R_{ac})	153.16	mΩ	55.23	mΩ



(a) Solution 1

(b) Solution 2

Fig. 9. The efficiency curves of the inductor design solutions, shown for different output voltages

VI. Conclusion

The paper presents an inductor design procedure to compare different design methods. Three design methods are presented and compared, and the design methods differ in the choice of core material and winding type. Ferrite cores and powder cores are used, along with copper foil and PCB as windings. The design methods are compared in two scenarios; the first with an output power of 10kW and the second with an output power of 20kW. In both scenarios, the design method using ferrite cores and PCB as windings, obtained the largest power density for the same efficiency, thereby being the most optimal design method for the given scenarios. For the same efficiency, the most optimal design method obtained up to 32% and 38% larger power density for the 10kW and 20kW scenario respectively, compared with the second most optimal design method. A design from both scenarios are presented where the most optimal design method are used. Both inductor designs obtain efficiencies of approximately 99.9% at half output power and maximum output current, which is the worst case operation point for a buck type inductor.

Acknowledgment

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