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Photo-induced and electrical degradation of organic field-effect transistors

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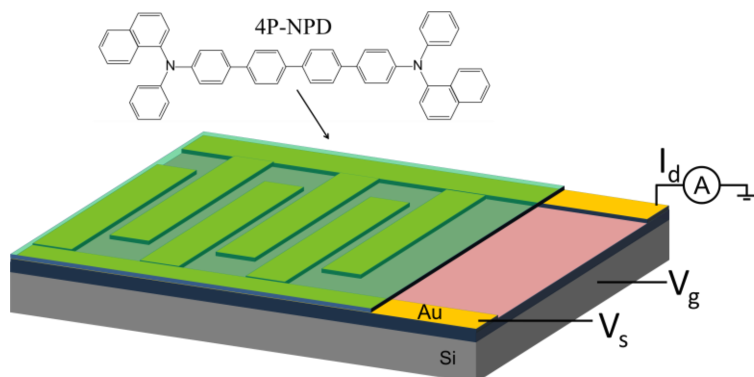
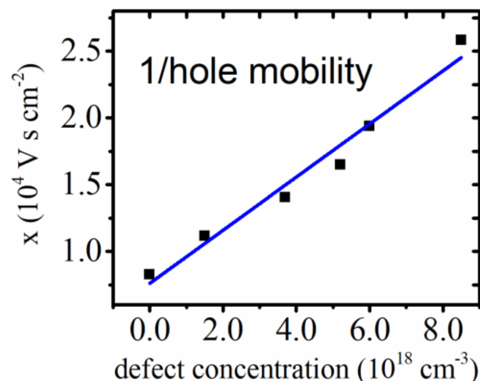
ABSTRACT

The field of organic field-effect transistors (OFETs) has matured over the past two decades and devices with charge carrier mobilities of several cm^2/Vs have been demonstrated. Nevertheless, to enter commercial products, the operational stability of OFET technology also needs to be addressed. Herein, two potential degradation mechanisms occurring in *N*,*N*'-di-1-naphthalenyl-*N*,*N*'-diphenyl [1,1':4',1'':4'',1'''-quaterphenyl]-4,4'''-diamine (4P-NPD)-based OFETs are investigated. Electrical transfer characteristics show that photo-induced oxidation of the organic thin-film decreases the hole mobility and increases the threshold voltage. The inverse hole mobility depends approximately linearly on the concentration of photo-induced defect states, which is in agreement with the Multiple Trapping and Release model. This implies that the created defects act as hole traps located energetically above the highest occupied molecular orbital level. In contrast, electrical stress increases the threshold voltage without affecting the hole mobility. This behavior is related to charge trapping, which probably take place in the gate dielectric as indicated by a relatively long trapping time of ~10^2 s. Time-resolved photoluminescence spectroscopy, which proved to be sensitive to both mobile and trapped charges, shows that the threshold voltage shift is caused exclusively by charge accumulation. The obtained results broaden the fundamental knowledge about the degradation processes occurring in OFETs, which is highly relevant for increasing their stability.





KEYWORDS

Degradation, 4P-NPD, photo-induced traps, organic field-effect transistor (OFET), time-resolved photoluminescence spectroscopy

HIGHLIGHTS

- Two degradation mechanisms occurring in OFETs are investigated
- Photo-induced degradation decreases hole mobility and shifts threshold voltage
- Photo-induced defects are identified as hole traps located above HOMO level
- Electrical degradation affects threshold voltage but not hole mobility
- Electrical degradation is caused exclusively by the charge accumulation
- Time-resolved photoluminescence can be used for investigating trapped charges

1 INTRODUCTION

During the last few decades, organic field-effect transistors (OFETs) have been studied intensively due to their potential in both scientific and technological applications [1–3]. Scientifically, the OFET platform is commonly used for investigating light emission [1] and charge transport properties of organic semiconductor materials [2,4]. Due to an improved understanding of the relationship between the molecular structure and its electronic properties, these findings promoted the development of new and improved organic compounds and related optoelectronic devices. Technologically, OFETs have the potential to become building blocks for a variety of inexpensive, light-weight and flexible electronic and optoelectronic devices including logic circuits [5,6], radio frequency identification tags [7,8], flexible displays [5,7], and chemical and biological sensors [9,10].

The field-effect mobility of novel organic semiconductor devices is comparable to the mobility found in conventional amorphous silicon and thin-film transistor technologies [2,11]. This has for example enabled the realization of an organic transistor backplane for display applications [12]. Inferior operational stability of OFETs, however, limits their application potential and suppresses rapid commercialization. OFETs degrade during their operation because of the applied electric field [13–15] but also due to extrinsic factors such as the presence of moisture [13,16–18], oxygen [19–21] and light exposure [21–23]. The degradation results in deterioration of the electrical device characteristics, which can be observed as a shift of the threshold voltage, a reduction of the field-effect mobility, or an increase of the OFF current [3]. The microscopic origin of these changes can be related to structural defects or chemical impurities within the organic material or at its interfaces, but this is in general not well understood.

In this work, we investigate two potential degradation pathways occurring in *N*,*N'*-di-1-naphthalenyl-*N*,*N'*-diphenyl [1,1':4',1'':4'',1'''-quaterphenyl]-4,4'''-diamine (4P-NPD)-based OFETs. Due to its high fluorescence quantum yield (~94%) and hole mobility of 6.6×10^{-4} cm^2 V^{-1} s^{-1} [24,25], this material has been used in several devices including: blue organic light-emitting diodes (OLEDs) as both the emitter and as hole transport material [26,27], white OLEDs as the blue emitter and the host material for triplet exciton harvesting [24,25], and organic solar cells as an exciton blocking hole transport layer [28]. First, we characterize the impact of photo-induced degradation on the electrical properties. Recently, we have used fluorescence lifetime measurements to investigate degradation mechanisms occurring in 4P-NPD films [29]. We found that the material is stable under the individual influence of ambient air or light exposure but undergoes a rapid degradation when illuminated with above-bandgap light under ambient conditions. This, in turn, leads to the formation of irreversible defect states acting as fluorescence quenchers, which indicate a photo-induced oxidation of 4P-NPD. While SiOH groups are formed on the SiO_2 surface under ambient conditions [30], the light exposure should not further influence neither the SiO_2 nor the gold layer, which allows us track the specific influence of the semiconductor material degradation on device performance. Subsequently, we use a combination of electrical studies and time-resolved photoluminescence (TR PL) spectroscopy to investigate the electrical degradation of the transistor when exposed to electrical stress. TR PL spectroscopy measurements serve as a selective characterization method sensitive to processes occurring in the semiconductor material and at its interfaces. Our results explain the influence of various degradation processes on the OFET performance, which is relevant for increasing their stability. Furthermore, they explain the impact of the photo-induced oxidation of 4P-NPD on its charge carriers transport properties and provide insights into the chemical nature of photo-induced defects states, which is highly relevant for other 4P-NPD-based optoelectronic devices.

2 EXPERIMENTAL METHODS

2.1 Sample fabrication

We fabricated bottom-contact bottom-gate OFETs on Si substrates. We used a highly N-doped, single-side polished Si wafer with an approx. 200 nm thick, thermally grown SiO_2 layer acting as the gate dielectric, while the Si substrate served as the gate electrode. On top of the SiO_2 layer, we patterned source and drain electrodes using negative photolithography, e-beam evaporation of titanium (3nm, adhesive layer) and gold (30 nm) followed by a lift-off process. In the applied design, which we present in Figure 1, the channel length and width were 10 µm and 8000 µm (8 interdigitated electrode gaps x 1000 µm, see Figure 1), respectively. Subsequently, we defined the contacts for the gate electrode by photolithography and etched through the SiO_2 with hydrofluoric acid, followed by deposition of 3 nm of titanium and 30 nm of gold and subsequent lift-off. Finally, we deposited 25 nm of 4P-NPD on top of the transistor substrates at rate of 0.2 Å/s via Organic Molecular Beam Deposition (OMBD). Afterwards, we immediately transferred the completed OFETs into a nitrogen-filled glovebox, where they were isolated from light.

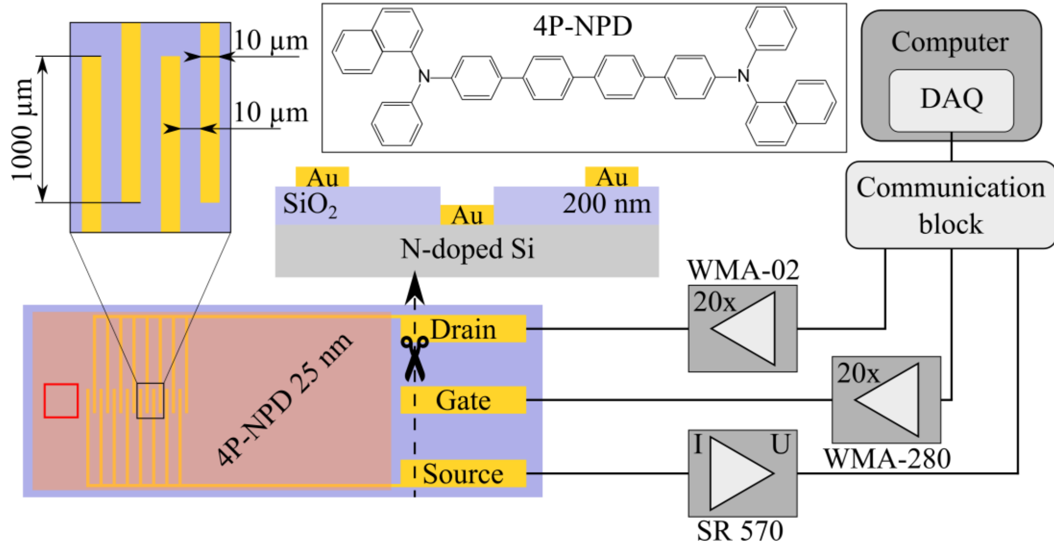


Figure 1 Design of the bottom-contact bottom-gate OFET and the schematic drawing of the setup for electrical characterization. Inset of the figure presents the molecular structure of 4P-NPD.

2.2 Electrical characterization

We characterized the electrical performance of the transistors using a custom-built, LabVIEW-based measurement system presented in Figure 1. The gate and drain voltages were supplied from a data acquisition card (National Instruments, PCI-6221) through two voltage amplifiers (Falco Systems, WMA-280 and WMA-02), while the current was measured via a current preamplifier (Stanford Research, SR 570). In this study, we measured the transfer characteristics in the saturation regime by sweeping the gate voltage between 0 V and -30 V (step size of 0.1 V) while keeping the drain voltage constant at -30 V. During the electrical characterization, we kept the transistors in vacuum (below 10^{-3} mbar) to minimize degradation.

2.3 Controlled degradation

We performed photo-induced degradation of the transistors by illuminating them under ambient conditions inside a solar simulator (Abet Technologies, Sun 3000 class AAA). The solar simulator provides white light (AM1.5G) with an intensity of 1 sun (100 mW/cm^2), which we periodically monitored using a calibrated reference cell (Oriel Instruments, 91150V). Upon the controlled degradation, we immediately transferred the transistors into the vacuum chamber for the electrical measurements, preventing any further degradation.

Secondly, we performed an electrical degradation of the transistors by subjecting them to electrical bias stress under ambient conditions. For that purpose, we utilized the previously described setup for electrical characterization, presented in Figure 1. We kept the transistor for 100 seconds under the electric load of -30 V applied to both the drain and the gate, while monitoring the source-drain current I_{ds}. We completed five such cycles for a total degradation time of 500 seconds. Additionally, we measured the transfer characteristics before and after each degradation cycle.

2.4 Optical characterization

We characterized the effect of the electrical degradation by means of TR PL spectroscopy using a custom-built, laser scanning microscopy (LSM) setup coupled with a streak camera system as detailed in [31]. The sample was excited at 395 nm wavelength, using the frequency-doubled output of a sub-100 fs Ti:Sapphire laser (Spectra Physics, Tsunami), with the repetition rate reduced by a pulse picker (APE, Pulse Select) to around 3.8 MHz. A microscope objective (Nikon, 40x, NA 0.65) was used to focus the laser beam onto the sample ensuring a diffraction-limited system resolution. We conducted all measurements under constant experimental conditions; 50000 exposures of 5 ms and constant slit opening. To prevent laser-induced degradation during the measurements, we kept the transistors in a custom-built vacuum chamber. We collected the signal from an area of approximately 120 µm x 120 µm using raster-scanning. Furthermore, we reduced the intensity of the laser using neutral density filters to prevent bimolecular events (e.g. exciton-exciton annihilation).

3 RESULTS AND DISCUSSION

Prior to any degradation experiments, we measured the electrical characteristics of the pristine transistor. The obtained results (black curve in Figure 2) showed a typical transistor behavior. For the first few measurements, we observed that the source-drain current slightly decreased with each consecutive measurement. Afterwards the current stabilized, and the following measurements induced only negligible changes. This measurement-induced, electrical degradation occurred even though the measurements were performed in vacuum. Storing the transistor in vacuum for around 1 h resulted in a partial recovery of the source-drain current indicating a reversible character of the degradation. We tested the magnitude of measurement-induced degradation by briefly venting the chamber and performing an additional series of measurements in vacuum. To allow a reliable comparison of the results, we always made a series of identical gate voltage sweeps and used the fourth measurement. As presented in Figure 2a, the measurement-induced degradation has a minor impact on the device performance. At the maximum gate voltage, the source-drain current dropped only by around 4 %. Nevertheless, it means that the transistor characteristics deteriorate during normal operation. The origin of the electrical degradation will be discussed in section 3.2, where we investigate the OFET performance under electrical load.

3.1 Photo-induced degradation of OFETs

Subsequently, we investigated the influence of the photo-induced degradation of the 4P-NPD thin-film on the transistor performance. We degraded the thin-film by illuminating the device in air for a cumulative time of 30 minutes. During this process, we repeatedly measured the transfer characteristics at different degradation stages. As shown in Figure 2a, the photo-induced degradation caused a significant decrease in the transistor current. During the first minute of degradation, the source-drain current (at V_g = -30 V) dropped by around 30 %, which is significantly higher than the measurement-induced changes. This suggests that the observed degradation is due to the photo-oxidation of the 4P-NPD thin-film. Furthermore, the transfer characteristics shift towards more negative values of the gate voltage while the slope in the on state decreases with degradation time. As a result, the current dropped down to around 23 % of its original value after 30 minutes of degradation. It is worth noting that while the on-state current decreases, the off-current remains unchanged, which leads to deterioration of the on/off ratio.

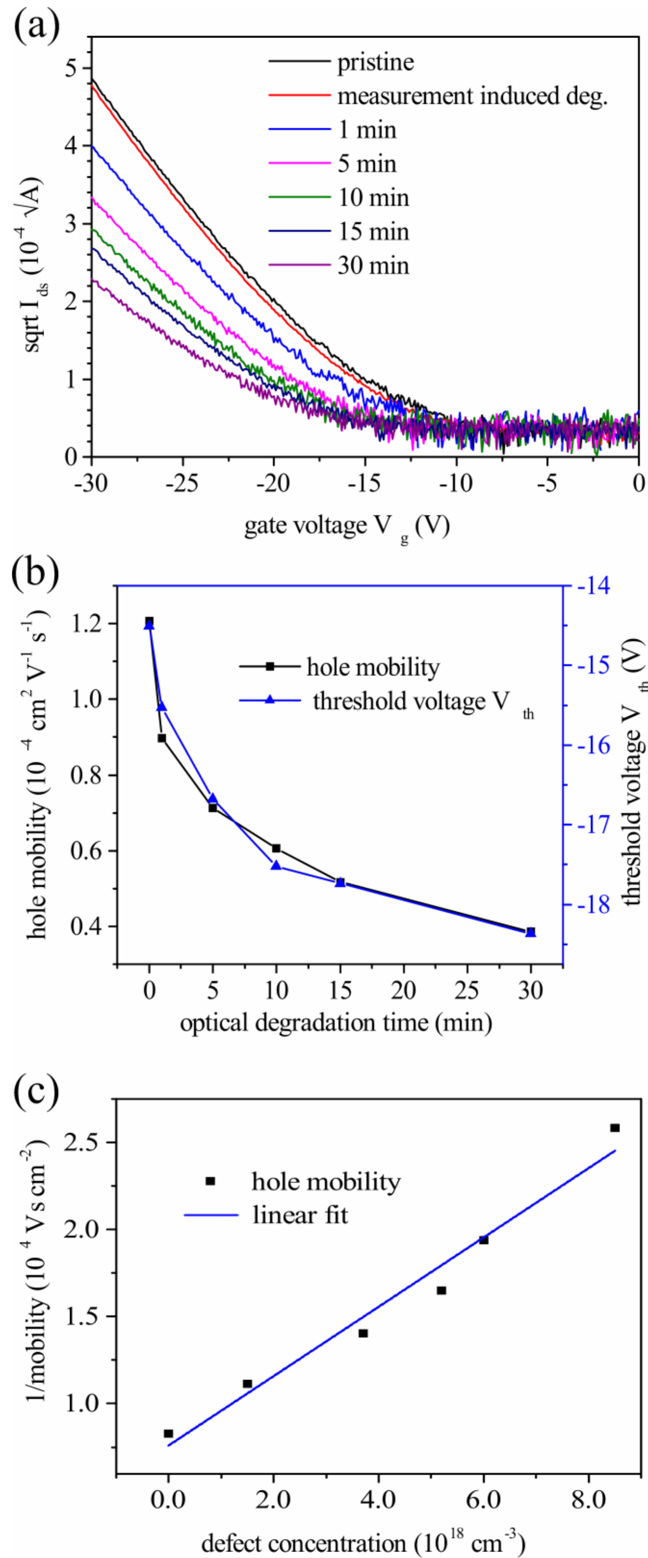


Figure 2 Changes in electrical characteristics of 4P-NPD-based OFET caused by photo-induced degradation. **a)** Transfer characteristics (forward sweep direction) at different photo-degradation stages. **b)** Field-effect hole mobility (black squares) and threshold voltage (blue triangles) versus degradation time **c)** Inverse of hole mobility versus concentration of photo-induced defects obtained from exciton diffusion Monte Carlo simulations [29].

3.1.1 Degradation-induced changes in the hole mobility and threshold voltage

We used the obtained transfer characteristics to determine the effective field-effect mobility of holes in 4P-NPD at different degradation stages. In the saturation regime the source-drain current I_{ds} is [1]:

$$I_{ds} = \frac{W}{2L}\mu_{sat} C_i \left(V_g - V_{th}\right)^2 \quad (1)$$

where L is the channel length, W is the channel width, μ_{sat} is the saturation mobility, C_i is the capacitance per unit area of the gate dielectric, and V_g and V_{th} are the gate and the threshold voltages, respectively. We determined the saturation mobility from the slope of the square root of I_{ds} vs. V_g curve in the on state. For the pristine device, we obtained a hole mobility of 1.2×10^{-4} cm^2 V^{-1} s^{-1}. This is smaller than the value of 6.6×10^{-4} cm^2 V^{-1} s^{-1} reported by Schwartz et al. for 4P-NPD [25]. However, in their studies, they performed measurements in a diode configuration with a thick (400 nm) 4P-NPD layer and extracted the mobility using the Mott-Gurney law, which may yield different mobility values [32]. Furthermore, it should be noted that the applied bottom-contact architecture as well as fringe currents from the electrode tips can introduce inaccuracies in our mobility measurements [33,34]. As shown in Figure 2b, the mobility decreased significantly with the degradation time. After 30 minutes, it dropped to around 0.4×10^{-4} cm^2 V^{-1} s^{-1}, which is only one third of the original value. Furthermore, we observed that the mobility decrease rate slows down as the degradation progress. During the first minute the hole mobility dropped by around 3.0×10^{-5} cm^2 V^{-1} s^{-1}. On the other hand, in the last measured degradation stage the mobility change rate was only 0.75×10^{-6} cm^2 V^{-1} s^{-1} per minute of degradation. The Multiple Trapping and Release (MTR) model describes charge transport in organic electronic devices as a dynamic process involving charge trapping in localized defect states (traps) and subsequent thermal release [35–38], which leads to the following expression for effective mobility μ:

$$\mu = \mu_0 \frac{N_c}{N_c + N_t} \quad (2)$$

where, μ_0 is the free carrier mobility in the absence of traps, and N_c and N_t are the concentrations of free and trapped charge carriers, respectively. The model thus predicts that the inverse mobility should scale with the total carrier density $N_{tot} = N_c + N_t$. In order to test this, we used results from our recent study [29], where we investigated the concentration of photo-induced defects in 4P-NPD films by means of exciton diffusion Monte Carlo simulations based on experimental time-resolved fluorescence data. The approximately linear relation between inverse mobility and defect concentration, seen in Figure 2c, indicates that the MTR model applies to our system.

Additionally, we determined the threshold voltage at different degradation stages by extrapolating the linear fit to source-drain current in the off-state. Many different effects contribute to the threshold voltage including built-in dipoles but also interface states and impurities creating charge traps, which have to be filled before the current can flow through the device [1,39]. Figure 2b shows the threshold voltage vs. degradation time, from which it is seen that the photo-induced degradation also has an impact on the threshold voltage, which shifted from around -14.5 V for the pristine transistor to approx. -18.5 V after 30 minutes of degradation. Similar to the hole mobility, the dynamics of the threshold voltage shift varies with the degradation time.

3.1.2 The nature of photo-induced defect states

We have previously shown that photo-oxidation of 4P-NPD leads to the irreversible formation of defect states, which act as fluorescence quenchers [29]. Nevertheless, we have not obtained any information about their chemical nature. Here, we show that, beside quenching the excitons, these defects also affect the hole transport properties. Considering this, the photo-induced defect states must be located near the highest occupied molecular orbital (HOMO). Both hole traps (states located above the HOMO level) and hole barriers (states located below the HOMO level) would affect the hole mobility by either immobilizing the carriers or increased scattering, respectively. However, according to our Monte Carlo simulations, the defect volume fraction, after 30 minutes of degradation, is as small as 0.45 %. Such a small fraction of barriers would not have a significant effect on the hole mobility, which in our case was reduced by two thirds. Based on this, we propose that defect states created during photo-induced oxidation of 4P-NPD are in fact the hole traps located above HOMO level, as illustrated in Figure 3.

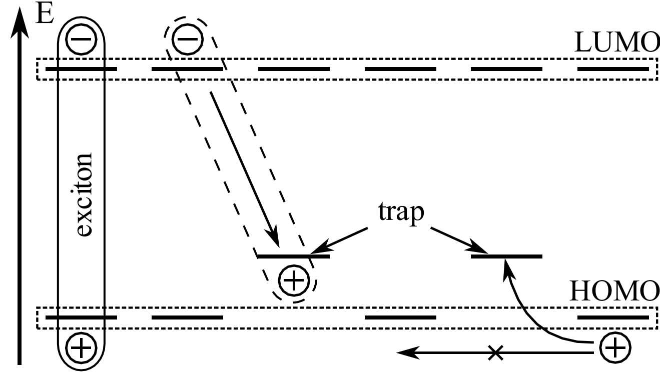


Figure 3 Energy diagram explaining the nature and the influence of photo-induced defects (traps) in 4P-NPD. On the left: the interaction of the trap with the exciton resulting in exciton quenching. On the right: the hole transferred between HOMOs of adjacent molecules being immobilized (trapped).

To further validate our finding, we have estimated the density of trapped charge carriers from the experimentally obtained threshold voltage shifts using the relation [40]:

$$\Delta V_{th} = -\frac{qN}{C_i} \tag{3}$$

where, q is the elementary charge, N is a surface density of the trapped charges and C_i is the gate dielectric capacitance per unit area. Using the experimentally obtained threshold voltage shifts, the relative dielectric constant of SiO_2 of 3.9 and assuming using a channel thickness of 1 nm for conversion from surface to volume trap density, we calculated the densities of trapped charges at all measured degradation stages [41]. In comparison to Monte Carlo simulation results, the calculated trapped charge densities (based on the measured threshold voltage shifts) are notably smaller but appear to have a similar functional form (Figure 4). We suggest that the observed discrepancy might be related to the differences between the two methodologies: Monte Carlo simulations determine the density of all defects, while Equation 3 considers only the density of trapped charges (filled defects). The current conduction in OFET is a dynamic process in which the charge carriers have a certain probability of being trapped and de-trapped. Therefore, only a fraction of the traps is filled at a given time. However, we note that the assumed channel thickness of 1 nm and consequently also the defect concentration found from the measured threshold voltage shifts are rough estimates. In reality, the charge carrier concentration in the channel decays rapidly with the distance from the interface without an actual well-defined channel thickness [42] causing the trap occupancy to vary in a similar manner. Considering this, our calculations are, at least qualitatively, in a good agreement with previously performed Monte Carlo simulations.

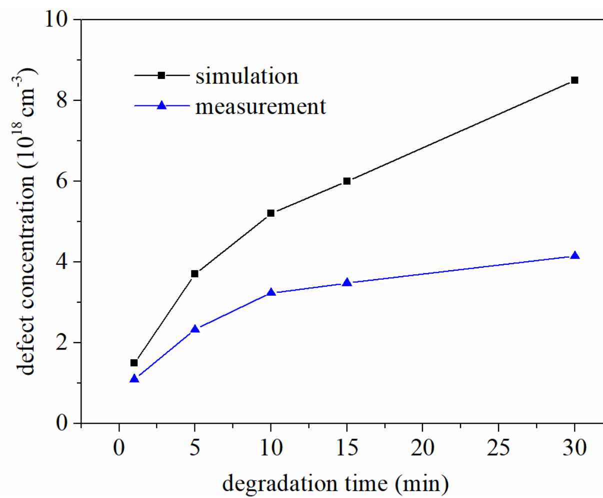


Figure 4 Comparison between the trapped charge density calculated from the experimental data (blue triangles) and the concentration of photo-induced defects obtained by means of Monte Carlo simulations (black squares) [29] at various degradation stages. Solid lines are guides for the eye.

3.2 Electrical degradation of OFETs

We investigated the influence of electrical bias stress under ambient conditions on the performance of 4P-NPD-based OFETs using a nominally identical device as before. Nonetheless, it exhibited an inferior performance as indicated by the electrical measurements (the lowermost curve in Figure 5a). After investigating the performance drop induced by a single measurement, we characterized the degradation caused by electrical stress by monitoring the source-drain current during five 100-second-long cycles (Figure 5b). Additionally, we measured the transfer characteristics before and after each cycle (Figure 5a). The obtained results, presented in Figure 5a, show that the electrical stress lead to significant reduction of the source-drain current. The current decreases less with each consecutive degradation cycle and it seems to stabilize after four cycles suggesting a saturation of the degradation process. Furthermore, as indicated by the horizontal lines in Figure 5b, the absolute current values at the beginning of each cycle are higher than at the end of the preceding one, which implies that the degradation process is, at least partially, reversible. Fitting the data obtained during the first degradation cycle yield an excellent agreement with a stretched-exponential function (see supplementary material), which is commonly used to describe current behavior under the bias stress [13,43]. This indicates that there is only one process involved in the electrical degradation.

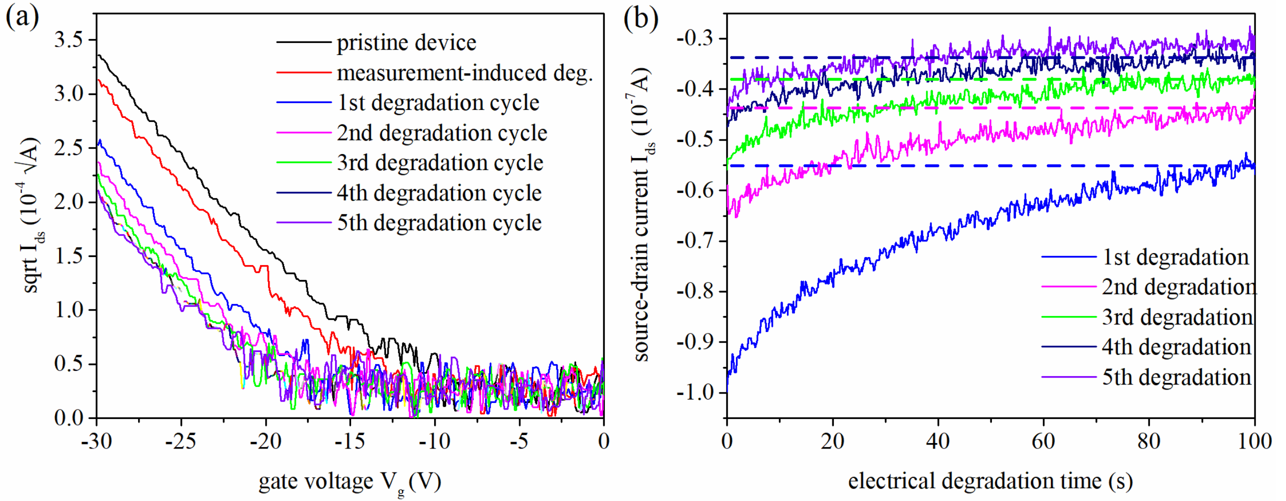


Figure 5 Degradation of 4P-NPD-based transistor induced by electrical stress a) changes in transfer characteristics (forward sweep) b) changes in source-drain current (at Vg = -30 V) as a function of degradation time. The dashed horizontal lines show the approximate current value at the end the degradation cycle marked with the same color.

The electrical stress has a qualitatively different impact on the transfer characteristics compared to the photo-induced degradation (Figure 2a). As shown in Figure 5a, the transfer curve shifts towards more negative gate voltages during the degradation process, while its slope in the on state seems to remain unchanged. Hole mobilities and threshold voltages extracted from the obtained transfer characteristics and presented in Figure 6 confirm that the mobility remains essentially unchanged under the electrical stress and the observed performance drop is caused solely by the threshold voltage shift. This behavior is typically ascribed to the trapping of charge carriers (holes) in localized trap states. Trapped holes contribute to the overall charge induced by the gate voltage however, since they are immobile, they do not contribute to the current causing the observed threshold voltage shift [3]. Such native or stress-induced traps can be located in the organic semiconductor, in the gate dielectric or at the semiconductor/gate dielectric interface [3,14,17,44]. Since the mobility remains unchanged during electrical bias, formation of additional defect states in 4P-NPD layer seems unlikely. On the other hand, the relatively long trapping time (~107 s) obtained from the fit (see supplementary material) suggests a barrier for the carriers to be trapped [45]. This could indicate that the traps responsible for the threshold voltage shift are located inside SiO_2, which is in agreement with previous studies of the exact location of the trapped charges in OFETs with SiO_2 gate dielectric [46].

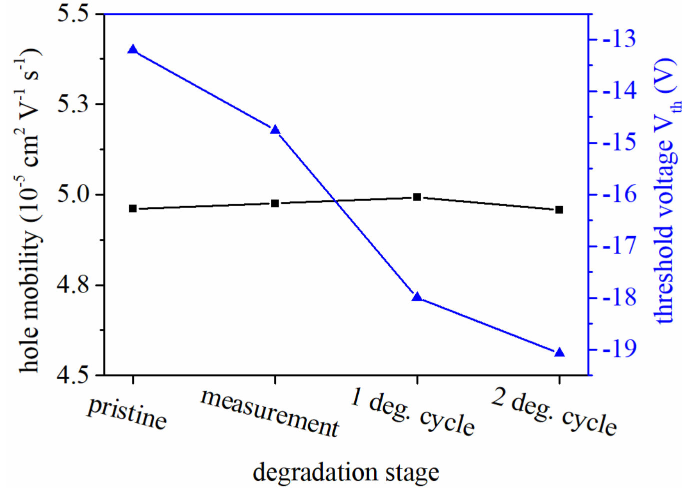


Figure 6 The influence of the electrical stress on the hole mobility and the threshold voltage of 4P-NPD-based OFET. Solid lines are guides for the eye.

3.2.1 Time-resolved photoluminescence studies of electrically degraded OFETs

We characterized the influence of the electrical degradation by means of time-resolved photoluminescence spectroscopy. It has been demonstrated that TR PL is sensitive to charge carriers because they act as exciton quenchers and the technique was successfully applied to map the charge carrier density in OFETs [42]. We measured the fluorescence decays from the pristine device (before any electrical characterization) and compared these with decays obtained after five cycles of the electrical stress. We performed the measurements over an area of approx. 120 µm by 120 µm in two distinct locations on the transistor: on top of the electrodes and transistor channel, and around 50 µm away from the electrodes, as indicated by a red square in Figure 1. The fluorescence decay obtained for the pristine OFET outside the electrodes is in close agreement with our previous studies showing a mono-exponential lifetime τ_1 of around 1.13 ns [29]. In contrast, the decay measured on top of the electrodes is clearly bi-exponential, which we ascribe to exciton quenching at the semiconductor-metal interface. By fitting the experimental decay with the longer lifetime component fixed to 1.13 ns, we obtained the shorter lifetime component τ_2, related to the quenching by electrodes, of around 0.28 ns. As shown in Figure 7, the electrical degradation reduced the fluorescence lifetime of 4P-NPD, which we attribute to exciton quenching by the holes remaining in the device. After the electrical degradation, the holes trapped during the process; even though they leave trap states after a short time, have no possibility to be harvested so they stay in the OFET for days. Therefore, in contrast to the electrical measurements (Figure 5b), showing a partial recovery of the characteristics, we did not observe any substantial lifetime changes in the consecutive TR PL measurements. This suggests that TR PL can be used to investigate not only mobile charge carriers during device operation [42] but also trapped carriers, which remain in the device after the degradation process. The observed degradation-induced changes in lifetime are relatively small because in OFETs, the current conduction in the organic channel occurs only in the close proximity (1-2 monolayers) to the gate dielectric interface [41,47,48]. Therefore, the excitons created in the upper parts of 25 nm 4P-NPD layer cannot reach the charge carriers because of their limited diffusion length (around 4.6 nm [27]). In contrast, the photo-induced degradation is a bulk process and it therefore affects the entire film thickness. Furthermore, we found that upon degradation the PL lifetime on top of and outside the electrodes changes in a similar fashion. In both cases, fitting the fluorescence decays using previously determined lifetimes resulted in an additional decay component τ_3 of around 0.71 ns. Nonetheless, we note that fitting three lifetime components may lead to a significant error in the absolute lifetime values. Similar degradation-induced lifetime components indicate that the source-drain voltage does not affect the degradation process. This is in agreement with the previous studies, which showed that the threshold voltage shift is caused solely by the gate voltage bias [13,14,49]. We conclude that the accumulation of charges, rather than the charge transport, is responsible for the degradation.

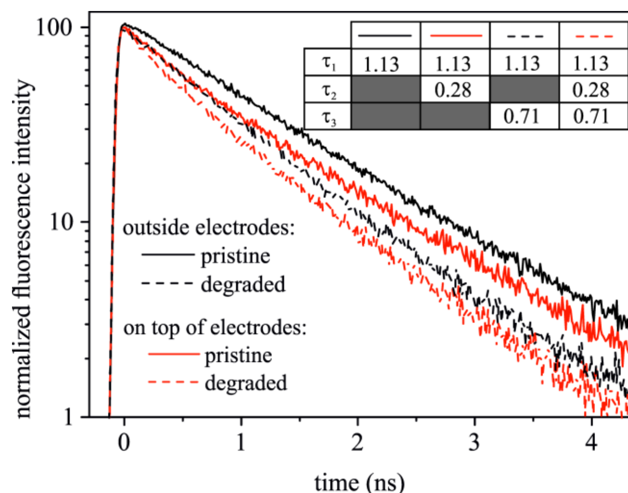


Figure 7 Changes in fluorescence decays of 4P-NPD induced by 5 cycles of the electrical degradation.

4 CONCLUSIONS

In summary, we investigated the influence of two potential degradation mechanisms occurring in 4P-NPD-based OFETs. We found that the selective photo-oxidation of a 4P-NPD thin-film results in a significant decrease of the hole mobility and increase of the threshold voltage. The approximately linear dependence between the inverse hole mobility and the concentration of irreversible defect states created during photo-induced degradation of the semiconductor is in agreement with the MTR model. The strong impact on the hole mobility and ability to quench excitons indicate that the defect states are, in fact, hole traps located above the HOMO level (within the HOMO-LUMO gap). Good agreement between trapped holes concentrations calculated based on measured threshold voltage shifts and defect concentrations obtained by Monte Carlo simulations further validate this finding. While investigating the impact of electrical bias stress on OFET characteristics we found that the electrical degradation increases the value of the threshold voltage, however, has essentially no effect on the hole mobility. Additionally, the electrical measurements revealed that the degradation process is at least partially reversible. We ascribe the observed degradation to trapping of the charge carriers. Fitting the current transient with a stretched exponential function yield a trapping time of around 10^2 s, which suggests that the traps responsible for the threshold voltage shift are located inside the gate dielectric. TR PL spectroscopy showed that this technique is sensitive to both mobile and trapped charges. We found that the degradation is caused by charge accumulation, rather than the current flowing in the channel. In other words, the source-drain voltage does not induce the electrical degradation, which depends exclusively on the gate voltage bias.

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